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A 12-bit ADC with independent gates for fast neutron spectrometry

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Abstract

We have developed a new integrating 12-bit analog-to-digital converter with independent gates. The circuit is especially designed for fast neutron spectrometry at very low intensity fields using multi-cell liquid scintillator detectors. A detailed layout and the main performances of the electronic circuit are described.

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1. Introduction

Liquid organic scintillator detectors are particularly suitable for fast neutron spectrometry because they offer the capability to determine the neutron energy spectrum by unfolding, by means of the response functions of the detector, the proton recoil pulse height distribution produced by neutron scattering [1,2]. Appropriate arrays of scintillator cells have been successfully used to measure low and very low neutron fields down to about 10^{-6} cm^{-2} s^{-1} [3,4], owing to their good capability in discriminating heavy-ionising particle interactions from electrons induced by the gamma-ray background. In this regard, a fast neutron passing through the sensitive volume of a liquid scintillator detector loses its energy mainly in elastic collisions with hydrogen atoms giving rise to proton recoils. The resulting thermal neutron can be captured by a neutron absorber (e.g. gadolinium, boron, etc.) which dopes the liquid scintillator or is itself a part of the detector structure (e.g. cadmium shields, lithium glasses, etc.). The neutron capture is followed by a cascade of energetic photons which may produce Compton electrons in the detector active volume. The signature of a neutron interaction in liquid scintillator is then one or more light pulses due to proton recoils followed by possible Compton electron signals.

In multi-cell neutron detectors the signal time sequence coming from photomultipliers on the

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different counters is random. Commercially available multi-channel analog-to-digital converters (ADC) are not designed to digitise asynchronous signal from their inputs, they require a gating pulse which triggers all the channel at the same time. The use of a single ADC per channel with its proper gating pulse is then required.

In this paper, we present a new integrating 12-bit ADC with independent gates, especially designed for the measurement of very low intensity neutron fields using multi-cell scintillator detectors. The board, which houses eight independent 12-bit current-integrating ADC channels, offers the capability to record multiple single spectra avoiding the necessity of external additional complicated electronics. The principle operation of the different electronic sections assembled in a VME module are described. Some test results are shown.

2. Principle of operation

As said before, the neutron interaction in multi-cell liquid scintillator detectors is characterised by the presence of "prompt" light pulses due to proton recoils which can be followed by "late" Compton electron signals. The time interval between prompt and late signals is fixed by the neutron thermalisation time. For fast neutron in liquid scintillator this time can be the order of tens of microseconds.

The proton recoil and Compton electron light pulses identification can be accomplished by means of pulse shape discrimination (PSD) techniques, based on the direct comparison of the fast and slow components of the light output from the scintillator [5]. To this purpose the digitisation and correlation, made on software level, between the total charge and the charge integrated after an appropriate delay ("delayed charge"), requires a series of well-timed gating signals and, in setting up in multi-cell detectors, the use of integrating ADC stages with independent gates.

In this regard, a simplified block diagram of a possible electronic set-up is given in Fig. 1. Let us consider an array of scintillator cells each one viewed by one photomultiplier (PMT). By means of signal splitters and passive delay lines, properly optimised for PSD, each PMT output feeds the analog inputs of two integrating ADC stages used for total and delayed charge sampling. A constant fraction discriminator (CFD) sets the minimum energy deposition and provides the proper gating signals for digitisation. For each event the main logic operation consists of setting a strobe logic level (Wait) in correspondence of the first prompt scintillation pulse and to wait for the possible coincidence of secondary pulses. For a neutron candidate event, defined by n prompt and m late signals, $2 \times (n + m)$ amplitudes are recorded:[1]

- n amplitudes for the prompt signals. One gets the neutron energy release by means of a spectrum unfolding.
- m amplitudes for the late signals. One gets the typical characteristic energy spectrum of the capture reaction.
- $n + m$ amplitudes (delayed charges) for the prompt and the late signals. One gets the proton–electron signal identification by means of pulse shape discrimination.

3. Circuit design

To lower the cost in large multi-cell detectors and simplify the electronic set-up, we have compactly mounted in a standard single-width 6U VME module (see Fig. 2) eight integrating ADC channels with their own gating circuits.

A block diagram of the electronics is shown in Fig. 3. Each channel, realised with basic ECL electronics, is build around a charge-to-amplitude converter (QAC) chip and a fast 12-bit ADC chip. An independent gating circuit (GC) provides the corresponding QAC with the proper integration time window every time an external ECL pulse

[1] We want to underline that the spectrum unfolding is affected by the order of storage of the data words. If this order is fixed by the proton recoil time sequence, one can use the same set of response functions to analyse the $n = 1$ and $n > 1$ events taking into account only the energy released in the first counter. On the contrary, if the neutron scattering order is not known, the set of response functions for the $n > 1$ events should be properly computed in order to take into account the contribution to the energy release coming from each counter.

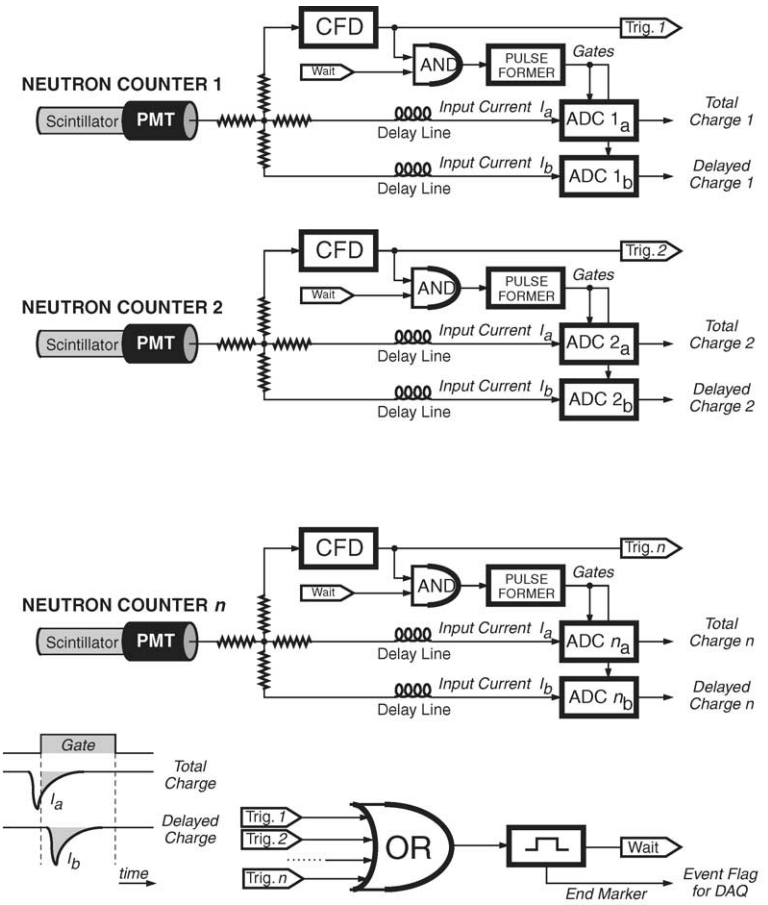

Fig. 1. Basic electronic set-up of a multi-cell liquid scintillator detector. The ADC timing for total and delayed charge measurement is shown.

triggers the circuit. Data are arranged in a FIFO memory 512×18-bit, readable via the VME bus. The correct timing and logic supervision of the electronics is provided by an internal Logic Control Unit (LCU) interfaced to the VME bus.

3.1. Charge-to-amplitude conversion

The function of charge integrator and voltage conversion (QAC) is carried out by the TSFL19319CCP integrated circuit developed in bipolar ASIC technology at the *Institut des Sciences Nucléaires de Grenoble* [6]. The main characteristics are summarised in Table 1.

Though two converters are integrated in a single monolithic chip, we have used eight chips (one per channel) in order to minimise any possible cross-talk between adjacent channels. The analog current that feeds the chip negative input (−IN) is diverted to a 100 pf capacitor (CEXT) whenever a positive logic level is presented at the chip gate input (G.IN). The capacitor voltage level V_C, proportional to the integrated charge Q, defines the QAC input sensibility:

$$V_C/Q = 10\ \mathrm{mV/pC}. \quad (1)$$

The voltage level V_C is kept stable by the chip and presented in output (V.OUT) for digitisation.

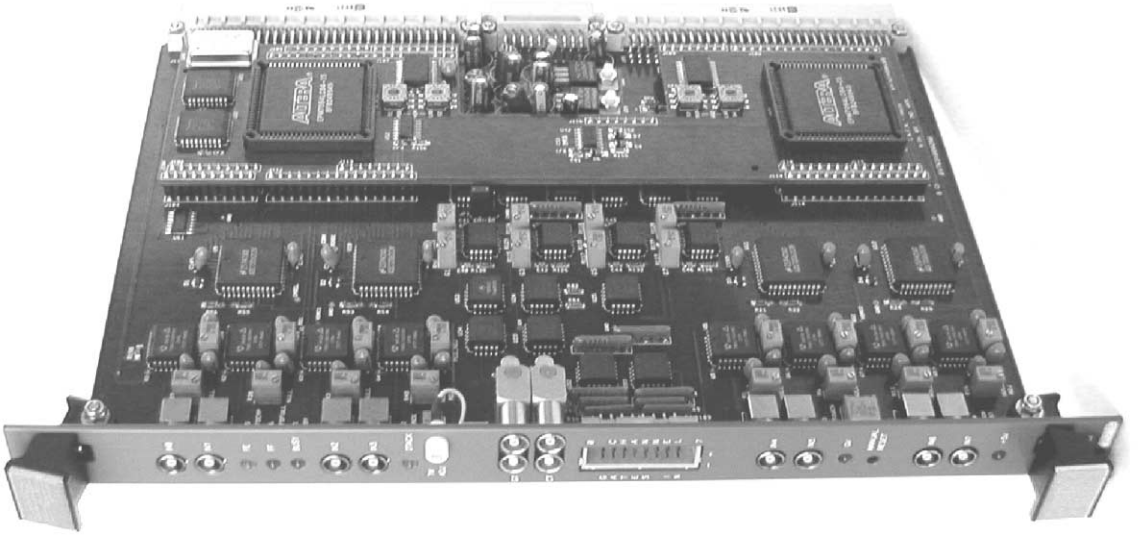

Fig. 2. The ADC board.

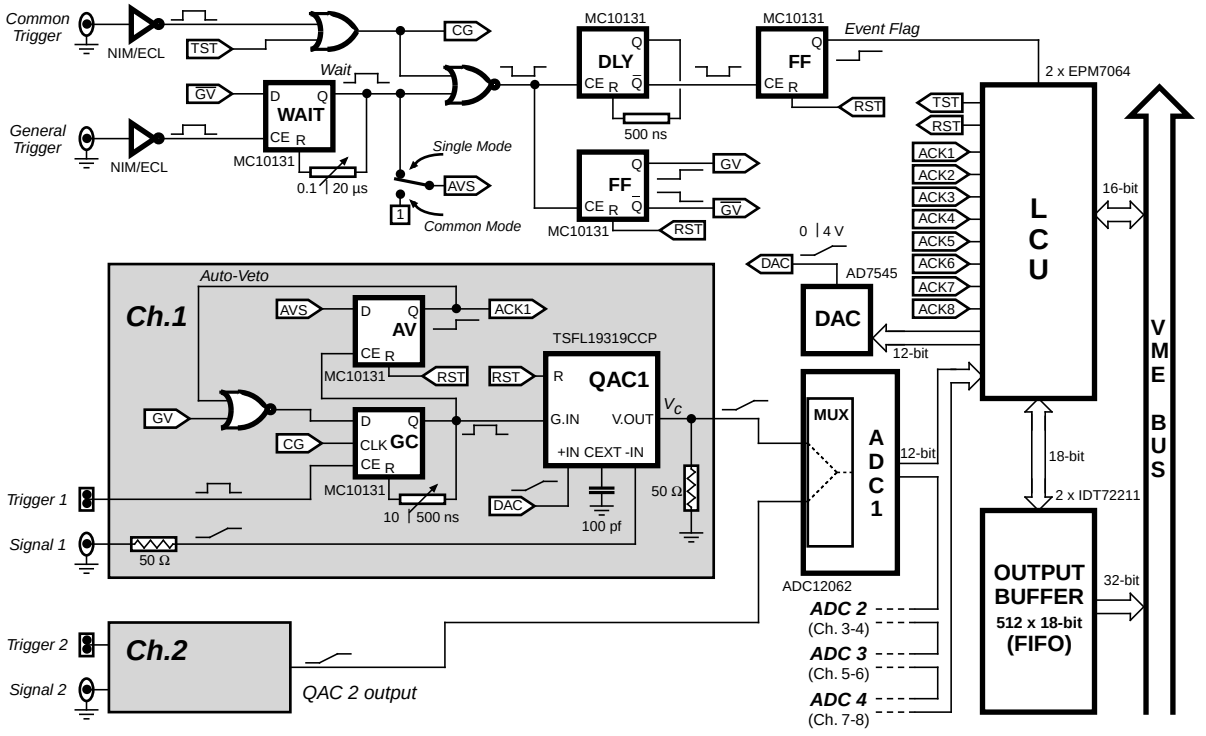

Fig. 3. ADC board electronics schematic.

Besides, the chip positive input +IN is directly fed by a 12-bit digital-to-analog converter (DAC) AD7545. Setting an internal register by means of the VME bus, the DAC provides a positive voltage level in the range 0–4 V. The DAC can be used to bias the input

Table 1
Main characteristic of the TSFL19319CCP chip [6]

Technology	ASIC
Chip type	28 pins LDCC
Analog channels per chip	2
I_{max} at the input −IN	100 mA
V_{max} at the input −IN	−5 V (over 50 Ω)
V_{max} at the input +IN	> 3 V
Signal-gate min. delay	<10 ns
Reset time	<200 ns
V.OUT range	0–5 V (over 50 Ω)
Max. conversion time	500 ns

current or to provide a software test for the eight QAC chips.

Each QAC is directly connected to an independent GC, physically realised with a D-type flip-flop MC10131 used in monostable configuration. The Q output provides the proper integration time window every time an external ECL trigger pulse is sent to the clock enable (CE) input. The time duration of the integration signal can be internally set in the range 10–500 ns. The eight gating circuits can also be simultaneously triggered by means of a common trigger pulse (CT) which feds the common clock (CLK) inputs of the MC10131 chips. The CT pulse can be generated for test purposes by means of a VME command. Lastly, providing the CT pulse by means of an external NIM pulse to the Common Trigger input, the board works in "common trigger mode" and carries out the normal operation of a common gate ADC module.

For each channel a simple pile-up rejection circuit (AV) is implemented by means of a D-type flip-flop MC10131. This, used in bistable configuration, carries out the veto function by means of a feedback line between the Q output and the D data input of the GC flip-flop. The gating circuit is inhibited by an *Auto-Veto* logic level after the generation of an integration signal and does not accept further trigger signals.

3.2. Sampling and digitisation

The sampling and digitisation of the voltage level at the eight QAC outputs is performed by means of four National Semiconductor ADC12062 integrated circuits. The main characteristics of the chips are summarised in Table 2 [7].

Table 2
Main characteristic of the ADC12062 chip [7]

Technology	CMOS
Operation	2 multiplexed channel
Dynamic range	12-bit
Sampling rate	1 MHz
Conversion time	740 ns
Sensibility	1 mV per count

Each chip has an input multiplexer that allows a 2 channel operation. The analog voltage at the multiplexer output is tracked and held by an internal sampling circuit and then is digitised using a 3 step flash technique. The input sensibility of the chip (1 mV/count) and its dynamic range (12-bit) allows the digitisation of the input level in the range from 0 V to 4 V. Taking into account the QAC performances, this corresponds to a full scale charge range of 400 pC and a resolution of 0.1 pC per ADC channel.

3.3. Timing and control

The LCU is the electronic circuit which carries out the logic control of the board and the data acquisition supervision. Based on two programmable logic devices (PLD) ALTERA EPM7064, the LCU is interfaced to the VME bus, to the ADC chips outputs and to the data output buffer. This last is realised with two 512×9-bit FIFO memories IDT72211 parallel connected in order to have 18-bit words.

The main functions carried out by the LCU are the following:

- It provides the general reset and clean of the different electronic stages of board;
- It can properly inhibit or enable the board by means of veto logic signals;
- It gives the correct timing and control signals for the data sampling and digitisation;
- It builds the data words to be transferred to the output buffer;
- It provides the interfacing to the VME bus;

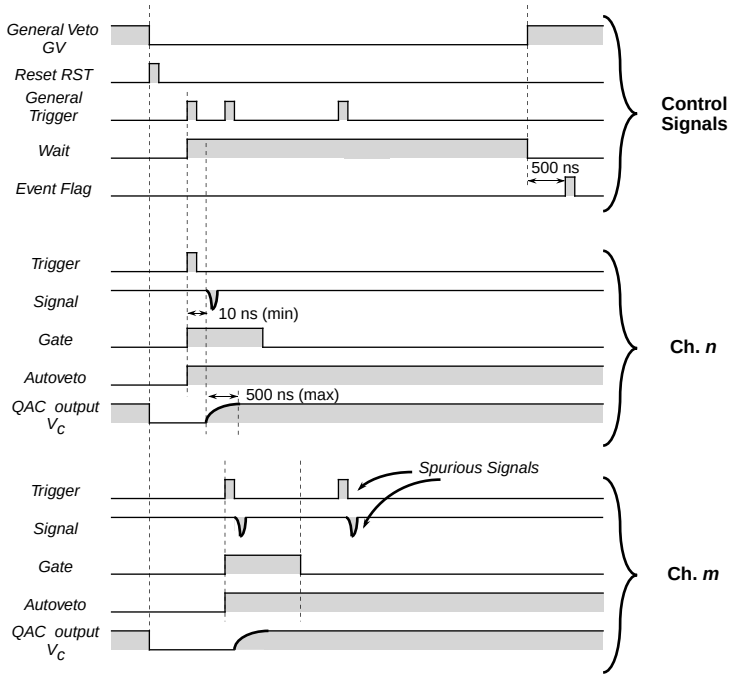

Fig. 4. Logic and timing sequence of an acquisition cycle.

- It provides some useful test functions.

The board can operate in two different mode depending on the status of a PLD control register settable by means of the VME bus.

- *Single-event acquisition mode*: the board is vetoed after the acquisition of an event and does not accept further trigger signal. The data acquisition restarts only after a VME clean command.
- *Multi-events acquisition mode*: data are automatically transferred to the output buffer till the FIFO memory is full.

The board is normally disabled by a General Veto logic level (GV) which inhibits the eight gating circuits. The GV is internally set by a D-type flip-flop MC10131 used in bistable configuration. The board is properly enabled by the LCU which changes the flip-flop state by means of an internal reset logic pulse (RST). Besides, the RST carries out simultaneously the eight QAC outputs clean and the veto reset of the eight gating circuits. In single-event acquisition mode the RST is provided by the LCU as a response of a VME command. In multi-events acquisition mode the RST is provided automatically by the LCU after the data transfer to the output buffer. In any case the RST can be triggered manually by means of a switch on the front panel of the board.

The logic and timing sequence of an acquisition cycle is shown in Fig. 4. The cycle is started providing the General Trigger input with a proper external NIM pulse. The pulse, converted to an ECL logic level, feds directly the input of a pulse former, physically realised with a D-type flip-flops MC10131 (WAIT) used in monostable configuration. This generates a timing delay (Wait) during which the input analog signals can be integrated supplying each channel with the proper ECL trigger pulse. The trailing edge of the Wait signal sets again the GV logic level and the board does not accept further trigger signals.[2]

[2] The Wait timing delay is not generated when the board operates in common trigger mode or when an internal trigger signal (TRT) is provided for test purposes. In these cases the AV circuits can be enabled setting the strobe line (AVS) to the logic state 1 by means of an internal jumper.

The duration of the timing delay can be set in the range 0.1–20 μs by means of a trimmer on the front panel of the board. At the end of the Wait delay a logic event flag for the LCU is generated.[3] This is used to increase the event counter register and to start the data sampling and digitisation phase. To this purpose the LCU checks, by means of eight acknowledge (ACK) logic lines, which channels have been triggered and present an output voltage level to be converted. The LCU drives the four ADC chip multiplexers and enables the digital conversion. If the corresponding ACK line is logically set, the digitised data are transferred to the output buffer.

Data in the FIFO memory are organised into "events" readable in VME D32 mode. Each event consists of a 32-bit header word followed by 0–8 32-bit data words. The header word includes the event counter and the event multiplicity, i.e. the number of triggered channels. Each data word includes the channel number and the corresponding converted value. The presence of data in the output buffer is pointed out by a PLD data-ready status bit. Data are transferred to the output buffer up to the full FIFO capacity. Then, a PLD FIFO-full status bit is set and the board is inhibited. A VME command cleans the output buffer and restarts the data acquisition.

4. Calibration and performances

The best performances in neutron spectrometry and pulse shape discrimination can only be attained properly calibrating the electronics in accordance to the scintillator type used for neutron detection. The light output from liquid organic scintillators consists of two, and possibly more, components each characterised by a different decay time defined by the properties of the scintillator chemical composition. The pulse shape discrimination is based on the direct comparison of the fast and slow components obtained by integration of the pulse shape over well-timed integration windows. Beside, the neutron thermalisation process, which sets the energy release in the detector and the signal time sequence from the different counters, depends on the detector geometry, on the scintillator density and on the H/C ratio.

[3] The additional 500 ns delay generated by the DLY flip-flop takes into account the QAC conversion time (≈ 500 ns) of the board when is used in common trigger or test mode.

Table 3
ADC test results

Integral non-linearity	$\pm 0.15\%$
Differential non-linearity	$\pm 0.5\%$
Full scale charge range	400 pC
Resolution	0.1 pC
Min. conversion time	1.8 μs

In the present case the board has been calibrated for the use of $2'' \times 6''$ cylindrical cells filled with the BICRON BC501A, which is almost universally adopted as reference liquid scintillator for fast neutron detection. The time duration of the eight integration windows are set to 300 ns in order to integrate almost all the main decay components of the scintillation light (3.16 ns, 32.3 ns, 270 ns) [8]. Besides the 10 μs fixed as time duration for the Wait signal is long enough to wait for the complete neutron thermalisation in a multi-cell detector [9].

Tests conducted to characterise the main ADC performances with the adopted calibration, confirm the correct functioning of the board. A few results are summarised in Table 3. In particular, for the differential non-linearity measurement, data have been accumulated adjusting the gating delay with respect to the general trigger pulse to fully cover the 10 μs fixed for the Wait signal. This test has been carried out to show a possible non-linearity concerning the QAC output that takes place after the complete integration of the input signal.

The study of the effectiveness of the actual ADC calibration in discriminating the neutron from the gamma ray field by means of pulse shape discrimination, a ^{252}Cf neutron source measurement has been performed using one of the above mentioned scintillator cells viewed by two 2 diameter EMI 9964KB03 photomultipliers. The experimental arrangement, shown in Fig. 5, which consents neutron interaction measurements in the range 0.5–20 MeV, makes use of a CAEN N715

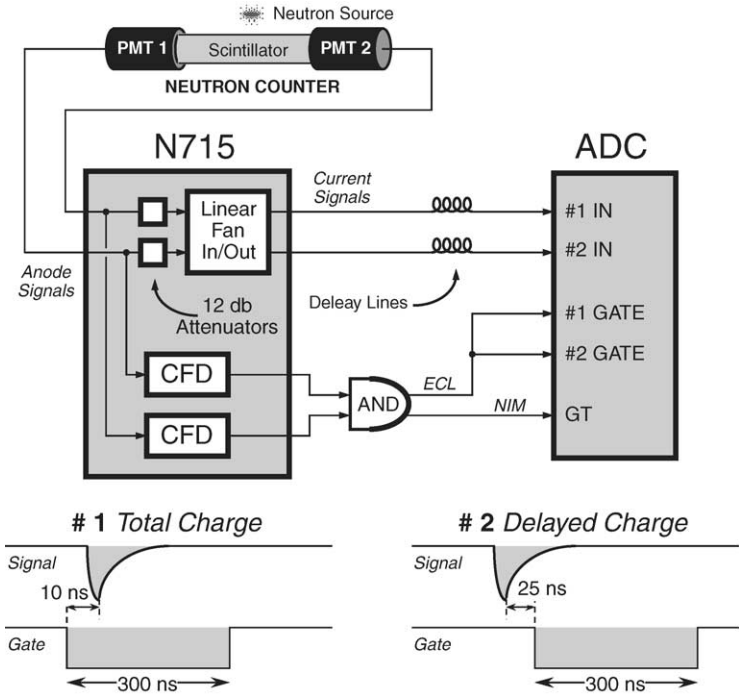

Fig. 5. Experimental arrangement used to measure the n–γ discrimination capability of the board. The time relation between the photomultiplier pulses and gates at the QAC inputs is shown.

"Dual PMT n–γ Discriminator" [10], in which is assembled almost all the necessary electronics, and two ADC channels, used as charge integrators for total and delayed charge measurement. The PMT outputs are connected to the inputs of the N715 module which attenuates (12 db) and sums up the anode pulses and feeds the two ADC analog inputs. The corresponding gating circuits are triggered by the coincidence signal coming from two constant fraction discriminator assembled in the N715 board, which set the minimum energy deposition of interacting particles. The coincidence signal, converted to a NIM pulse, is also used as *General Trigger* to enable the ADC board. The adopted relation between the PMT pulses and triggers at the ADC inputs is shown in lower part of Fig. 5.

Fig. 6 presents the typical two-dimensional spectrum of the delayed charge versus the total one. The plot is characterised by the presence of two well-separated branches for gamma-ray and neutron interactions. The result shows the good efficiency and resolution performance of the electronics set-up in the neutron identification and a very effective gamma-ray rejection, by a factor of about $1{:}10^5$ down to about 50 keV energy of recoiling electrons.

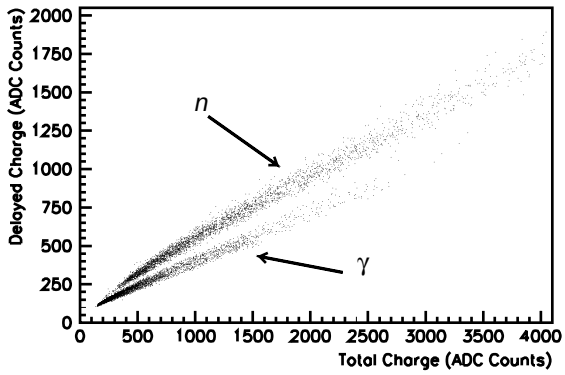

Fig. 6. Two dimensional spectrum of the delayed charge versus the total one measured with a Cf neutron source.

We want to underline that spurious background counts, due to the presence of possible nuclear contamination in the liquid scintillator (mostly alpha emitters), can bypass this discrimination logic [3]. For this reason, for very low neutron field measurements, one requires a more specific neutron signature based on neutron multiple scattering or capture gamma-ray spectrometry.

5. Conclusion

A new 12-bit integrating ADC board with independent gates has been developed. The device offers the possibility to set-up a compact and low cost electronics for multi-cell neutron detectors. The high dynamic range, the good resolution, the capability to record multiple single spectra and the possibility to perform a capture gamma-ray spectrometry, make this device a very promising tool for the realisation of big multi-cell spectrometers able to measure very low neutron fields.

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