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CMOS MAPS upgrade for the Belle II Vertex Detector

M. Babeluk[a], M. Barbero[b], J. Baudot[c], T. Bergauer[a], F. Bernlochner[d], S. Bettarini[e,f], F. Bosi[e,f], Y. Buch[g], G. Casarosa[e,f], J. Dingfelder[d], T. Fillinger[c], C. Finck[c], A. Frey[g], C. Hu[c], C. Irmler[a], C. Marinas[h], M. Massa[e,f], L. Massaccesi[e,f], M. Minuti[e,f], H. Pham[c], G. Rizzo[e,f], C. Schwanda[a], B. Schwenker[g], M. Schwickardi[g], C. Wessel[d,*], on behalf of the Belle II VTX collaboration

[a] *Institute of High Energy Physics, Austrian Academy of Sciences, 1050 Vienna, Austria*
[b] *Aix Marseille Université, CNRS/IN2P3, CPPM, Marseille, France*
[c] *Université de Strasbourg, CNRS, IPHC, UMR 7178, Strassbourg, France*
[d] *University of Bonn, Bonn, Germany*
[e] *INFN Sezione di Pisa, Pisa, Italy*
[f] *Dipartimento di Fisica, Universià di Pisa, Pisa, Italy*
[g] *II. Physikalisches Institut, Georg-August-Universitaet Goettingen, Goettingen, Germany*
[h] *IFIC - Instituto de Física Corpuscular (CSIC/University of Valencia), Valencia, Spain*

Abstract

The success of the Belle II experiment in Japan relies on the very high instantaneous luminosity, close to $6 \times 10^{35}\text{cm}^{-2}\text{s}^{-1}$, expected from the SuperKEKB collider. The corresponding beam conditions at such luminosity levels generate large rates of background particles and creates stringent constraints on the vertex detector, adding to the physics requirements. Current prospects for the occupancy rates in the present vertex detector (VXD) at full luminosity fall close to the acceptable limits and bear large uncertainties. In this context, the Belle II collaboration is considering the possibility to install an upgraded VXD system around 2027 to provide a sufficient safety margin with respect to the expected background rate and possibly enhance tracking and vertexing performance.

The VTX collaboration has started the design of a fully pixelated VXD, called VTX, based on fast and highly granular Depleted Monolithic Active Pixel Sensors (DMAPS) integrated on light support structures.

The two main technical features of the VTX proposal are the usage of a single sensor type over all the layers of the system and the overall material budget below 2 % of radiation length, compared to the current VXD which has two different sensor technologies and about 3 % of radiation length. A dedicated sensor (OBELIX), taylored to the specific needs of Belle II, is under development, evolving from the existing TJ-Monopix2 sensor. The time-stamping precision below 100 ns will allow all VTX layers to take part in the track finding strategy contrary to the current situation. The first two detection layers are designed according to a self-supported all-silicon ladder concept, where 4 contiguous sensors are diced out of a wafer, thinned and interconnected with post-processed redistribution layers. The outermost detection layers follow a more conventional approach with a cold plate and carbon fibre support structure, and light flex cables interconnecting the sensors.

This document will review the context, technical details and development status of the proposed Belle II VTX.

Keywords: Belle II, VXD, SVD, PXD, VTX, Upgrade, CMOS, DMAPS

1. Introduction

The Belle II experiment [1] located at KEK in Tsukuba, Japan, is an all-purpose full solid angle particle detector. It records data from collisions at the interaction point of the asymmetric e^+e^- SuperKEKB collider [2], which operates at a centre of mass energy of $\sqrt{s} = 10.58\,\text{GeV}$, corresponding to the mass of the $\Upsilon(4S)$ resonance, which decays into two B mesons in nearly 100 % of all cases. To fulfill the physics requirements of Belle II the vertex detector (VXD) is an essential part of the system. However, the SuperKEKB team is working on improvements to the final focusing magnets and the interaction region to be able to achieve the target luminosity. Because of this, it might be necessary to change the position or the shape of the final focusing magnets, or both, potentially resulting in a redesign of the interaction region. In case of substantial changes of the interaction region, the VXD likely cannot be kept and a new detector will be necessary, independent of the hit rates and radiation environment. To ensure safe operation of the experiment while guaranteeing high tracking and vertexing performance towards the high luminosity of $6 \times 10^{35}\text{cm}^{-2}\text{s}^{-1}$, the VTX collaboration is developing a new fully pixelated CMOS detector to replace the VXD in the timescale of 2027 [3]. This new detector is one of four proposals for the (partial) replacement of the VXD; the other three proposals are a new DEPFET pixel detector as replacement for the current DEPFET based PXD, a refined strip detector with smaller strip pitch in z direction and a reduced sensor thickness as replacement for the current strip detector, and a silicon on insulator pixel detector to cover the full VXD volume similar to the VTX.

The remaining part of this document first introduces the con-

*Corresponding author
Email address: christian.wessel@desy.de (C. Wessel)

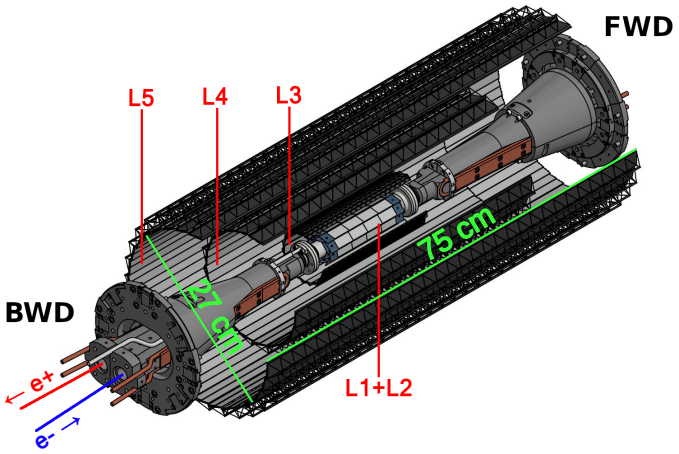

Figure 1: A CAD rendering of the VTX layout. The baseline concept contains 5 straight barrel layers filling the current VXD volume.

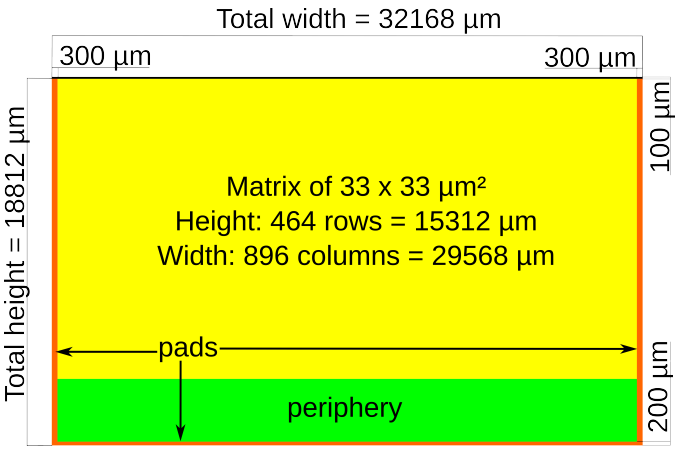

Figure 2: Design schematic for the OBELIX chip.

cept of the VTX and the underlying technology in Section 2, followed by a conclusion and outlook to further developments in Section 3.

2. Concept of the VTX

In its innermost part, the Belle II experiment is currently equipped with two layers of DEPFET [4] pixels (PXD) at radii of 1.4 and 2.2 cm, and four layers of double sided silicon strip sensors (SVD) [5] at radii between 3.9 and 13.5 cm, which together form the VXD, which corresponds to the configuration defined in the technical design report for Belle II. Its main task is the precise estimation of decay vertices in addition to very low momentum track finding. The VXD is surrounded by the central drift chamber (CDC) as the main tracking device, ranging from 16 cm to 112 cm in radius. The PXD is also needed to be able to resolve the vertices of decaying B mesons to enable measurements of oscillation of neutral B mesons, which requires the resolution of the impact parameters d_0 and z_0 to be in the order of 10 µm. As the difference in flight length between both particles is only about 150 µm due to a boost of $\beta\gamma = 0.28$ caused by the asymmetric beam energies of 7 GeV (4 GeV) of the electrons (positrons), a highly granular vertex detector is mandatory.

To achieve the target instantaneous luminosity, the nano beam scheme [6] is used. While the vertical beam size already is reduced significantly to previous accelerators and experiments, further reduction is foreseen for the next years to shrink the beam size in the interaction point to tens of nm in the vertical direction. This requires strong focusing of the beams, resulting in large amounts of beam induced backgrounds, which especially affects the VXD as the innermost detector.

The goal of the VTX is to develop a fully pixelated detector based on Depleted Monolithic Active Pixel Sensors (DMAPS) using industry standard CMOS processes, which is foreseen to replace the full VXD after 2027. The currently proposed concept includes five layers using sensors based on the TowerJazz 180 nm process, as depicted in Figure 1. The figure shows the central beam pipe surrounded by the two innermost layers (called *iVTX*) in the centre at radii of 1.4 and 2.2 cm, which are followed by the three outer layers (called *oVTX*) at radii of 3.9, 9, and 14 cm. The radii and the number of layers are not yet final but need further studies for optimisation. Low material budget is essential, as the particles in Belle II are very soft, thus multiple Coulomb scattering needs to be minimised. Considering the high background level expected in the VTX, with hit rates up to 120 MHz/cm^2 in the innermost layer, corresponding to TID of 10 Mrad/year and NIEL of 5×10^{13} n$_{eq}$/cm^2/year, the expected power consumption of the fast DMAPS chip under development will be about 200 mW/cm^2.

In the VTX design we plan to have a material budget of 0.1 % X_0 for the two innermost layers, about 0.3 % X_0 for the two following layers and about 0.8 % X_0 in the outermost layer. In order to achieve the very low material budget, the two innermost layers are designed to be self-supported air cooled all-silicon ladders, while the three outer layers are water cooled and on a carbon fibre structure for support, which is also visible in Figure 1.

The sensor size is foreseen to be 3×2 cm^2, with pixel pitches of 30 µm to 40 µm in both directions. The sensor under development, called OBELIX, is derived from the existing TJ-Monopix2 chip [7, 8]. Several different front end flavours exist, and the final decision on one flavour has not yet been made. Timestamp clock signals of down to 25 ns can be used to be able to cope with the target hit rate of 120 MHz/cm^2.

Compared to the TJ-Monopix2, which features a triggerless architecture with no memory on the periphery, the digital logic needs to be adapted to fit the needs of Belle II. OBELIX will have a triggered readout architecture, with a fixed latency of about 5 µs, and will be operated up to 30 kHz trigger rate. With the foreseen short acquisition window of about 100 ns, we can limit the data throughput to 320 Mbps, even with the high target hit rate expected. A schematic layout of the OBELIX chip is shown in Figure 2. The active area of about 3×1.5 cm^2 covers the main part of the chip. In the periphery an additional

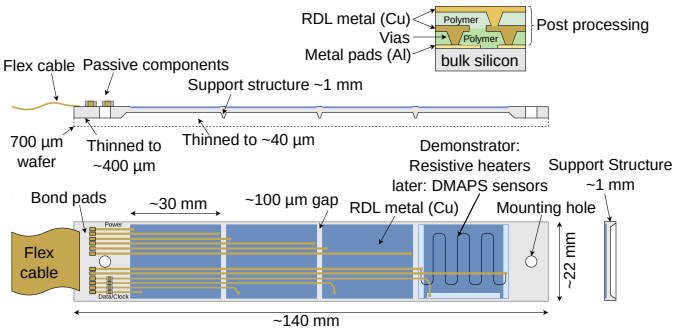

Figure 3: Sketch of the all silicon ladder concept of the iVTX. Four dummy sensors with a length of about 30 mm are shown in blue on the silicon support structure (grey) with a width of about 22 mm and a length of about 140 mm. The yellowish lines indicate power and data transition lines, one line of both to each chip. Power is supplied to the ladder by a flex cable (left), which also transmits data to and from the chips in for the final chips.

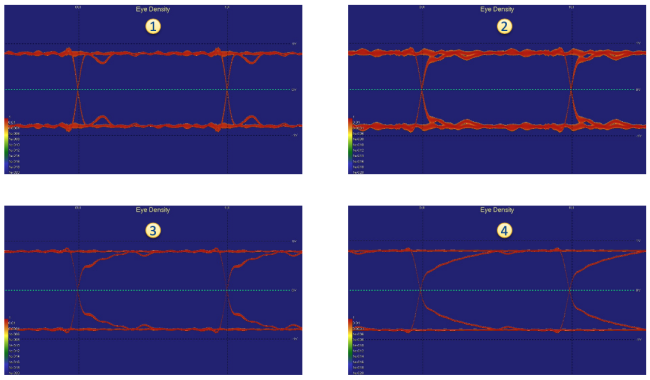

Figure 4: Eye openings of the iVTX data transmission lines at four different positions on the ladder.

area of about 3×0.3 cm^2 is required for data (pre-)processing and triggering as well as LDO regulators, data transceiver, and monitoring circuits. A first design prototype of the new chip will be submitted in autumn 2022.

2.1. First iVTX demonstrator

Figure 3 shows a schematic drawing of the iVTX demonstrator ladder with an overall length of about 140 mm and a width of about 22 mm. Instead of actual sensors the ladder is equipped with four dummy chips with integrated surface resistors. These resistors are used to mimic the estimated heat load in order to test the cooling concept. In addition, it is also equipped with redistribution layers (RDL) for power and data to connect every chip with the flex cable at the end of the ladder. The sensitive areas are thinned down to about 40 µm to test the mechanical integrity of the assembly and to develop the thinning process. The overall support is provided by the remaining thicker frame around the active area.

Signal quality at the far end, power delivery, and the full assembly process are to be tested. Eye diagrams from simulation with a transfer rate of 640 Mbps are depicted in Figure 4, indicating that data rates of 320 Mbps will be possible.

Figure 5: Prototype of the layer 5 truss, which is the longest truss. It is made from thin carbon fibre structures and evolved from the ALIC ITS2 space frame concept.

Figure 6: First prototype of the cold plate. The figure only shows one end. One coolant tube (golden) is connected to the cold plate (black) and turns 180° on the other end (not shown) so that the coolant flows both directions and thus leaves on the same side it starts.

In total five demonstrators can be produced on a 200 mm wafer. First thinned multi-chip CMOS demonstrator ladders have been produced and characterised with different thickness and geometries, showing a homogeneous thickness over an area of 10 cm^2.

2.2. oVTX development

The oVTX is not self-supported, as the distance required to cover the acceptance is too large, the mechanical integrity is provided by a carbon fibre support structure called *truss*, as depicted in Figure 5. This structural design evolved from the ALICE ITS2 space frame concept [9]. With a length of 70 cm and a weight of only 5.8 g it is able to carry more than 40 sensors in two rows next to each other with a small overlap, achieving a very low material budget. In order to cool the sensors a cold-plate concept is in development, as shown in Figure 6. The sensors are glued to the cold-plate, which is then mounted to the truss. For each sensor row, a polyimide cooling tube runs over all sensors and turns back at the other end, such that the heated coolant leaves on the same side. Depending on the thermal testing, it will either be guided back to the cooling system, or fed into another ladder.

An explosion drawing of a fully assembled layer 5 ladder is shown in Figure 7. In addition to the carbon fibre structure (bottom), two cold plates for the two neighbouring sensor rows are

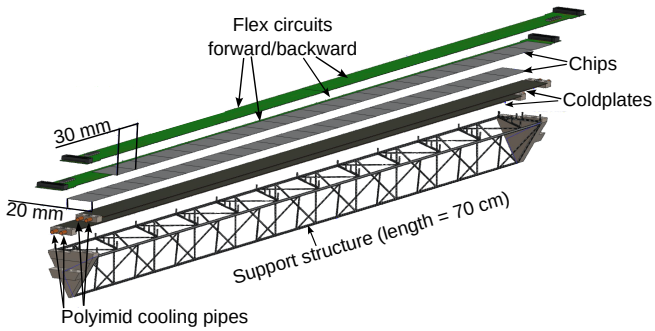

Figure 7: Explosion drawing of a fully assembled layer 5 ladder.

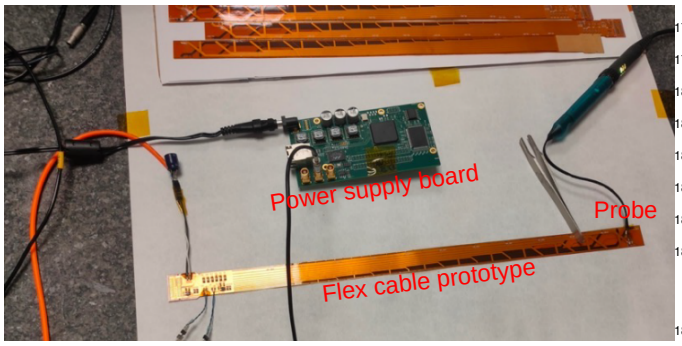

Figure 8: Test of the oVTX transmission line signal integrity.

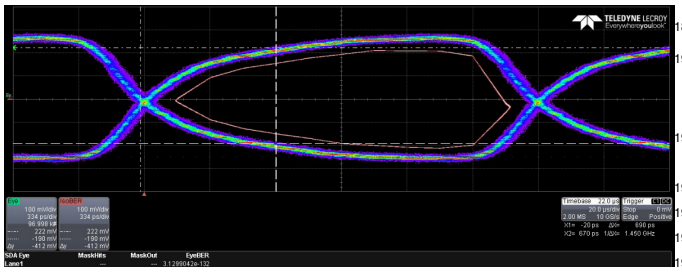

Figure 9: Eye diagram for the oVTX transmission line signal integrity of the layer 5 flex cable.

shown, as well as the flex cables for power and data transmission (top). With the truss assembled, first thermo-mechanical tests were performed. These first tests demonstrated that the first resonance frequency is at 200 Hz, which is above the frequencies of typical earthquakes in Japan, and that the thermal properties are good.

Since the transmission lines and the flex cable need to be as thin as possible, but also need to ensure save data transmission, the 70 cm long outermost ladders are equipped with two flex cables per ladder, one from each side of the truss. Figure 8 shows the setup to test the signal integrity of one of the 35 cm long transmission lines for data transmission rate of 500 Mbps. The signal is injected on the left side and read out on the right side. The resulting eye diagram of the measurement is shown in Figure 9. A clear difference between high and low can be seen, indicating an excellent signal integrity for the 35 cm long flex, providing a good starting point for further developments.

3. Conclusion and outlook

The necessary changes to the SuperKEKB interaction region in the core of the Belle II detector might alter the detector boarder, which could make it impossible to keep the current VXD in place. In order to prepare for this scenario, and to cope with potentially high occupancies, the VTX project was started, aiming for a pixelated all-CMOS replacement of the VXD. While simulations indicate substantial improvements in the tracking and physics performance with a five layer CMOS pixel detector replacement for the VXD [10], the development and testing of the VTX is ongoing. Low material budget fitting the needs of the Belle II experiment can be achieved, as well as high signal integrity and sufficient cooling for the expected 200 mW/cm^2 of dissipated power. As a final goal, low power OBELIX chip suiting the needs of Belle II is developed alongside the necessary infrastructure for power delivery, readout, and cooling. The VTX collaboration will contribute to a conceptual design report for the Belle II upgrade by early 2023 and continue to work on testing and developing the system, aiming for installation in 2027.

4. Acknowledgment

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