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Nuclear Instruments and Methods in Physics Research A 533 (2004) 178–182
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

Design aspects and prototype test of a very precise TDC system implemented for the Multigap RPC of the ALICE-TOF

A.V. Akindinov[a], A. Alici[b,c], F. Anselmo[b], P. Antonioli[b,*], M. Basile[b,c], G. Cara Romeo[b], L. Cifarelli[b,c], F. Cindolo[b], F. Cosenza[d], I. D'Antone[b], A. De Caro[d], S. De Pasquale[d], A. Di Bartolomeo[d], M. Fusco Girard[d], V. Golovine[a], M. Guerzoni[b], M. Guida[d], D. Hatzifotiadou[b], A.B. Kaidalov[a], D.H. Kim[e], D.W. Kim[f], S.M. Kisselev[a], G. Laurenti[b], E. Lioublev[a], K. Lee[f], S.C. Lee[f], M.L. Luvisetto[a], A. Margotti[b], A.N. Martemiyanov[a], F. Massera[b], S. Meneghini[b], R. Michinelli[b], R. Nania[b], P. Otiougova[e], G. Pancaldi[b], A. Pesci[b], R. Pilastrini[b], O. Pinazza[b], P.A. Polozov[a], M. Rizzi[b], E. Scapparone[b], G. Scioli[b,c], S. Sellitto[d], F. Semeria[b], A.V. Smirnitski[a], M.M. Tchoumakov[a], E. Ugolini[b], E. Usenko[g], G. Valenti[b], K.G. Voloshin[a], M.C.S. Williams[b], B.V. Zagreev[a], C. Zampolli[b,c], A. Zichichi[b,c], M. Zucchini[b], M. Zuffa[b]

[a]*Institute for Theoretical and Experimental Physics, Moscow, Russia*
[b]*Istituto Nazionale di Fisica Nucleare, Bologna, Italy*
[c]*Dipartimento di Fisica dell'Università, Bologna, Italy*
[d]*Dipartimento di Fisica dell'Università and INFN, Salerno, Italy*
[e]*World Laboratory, Lausanne, Switzerland*
[f]*Department of Physics, Kangnung National University, Kangnung, South Korea*
[g]*Institute for High Energy Physics, Protvino, Russia*

Available online 28 July 2004

*Corresponding author. University of Bologna & INFN-Bologna, Via Irnerio, 46, Bologna 40126, Italy.
E-mail address: antonioli@bo.infn.it (P. Antonioli).

0168-9002/$ - see front matter
doi:10.1016/j.nima.2004.07.023

Abstract

The ALICE Time-of-Flight system will be a large area (150 m^2) detector made by Multigap RPC (MRPC). T he time digitisation is based on the High Performance TDC chip (HPTDC). Tests carried out on board prototypes are discussed, emphasising the optimisation of the effective time resolution of the chip when working in its Very High Resolution Mode. Lab bench tests and test beam results show that a 20 ps resolution has been achieved.

PACS: 29.40.Cs; 84.30.−r; 84.30.Sk

Keywords: Resistive plate chambers; ALICE; Time of Flight; Time resolution; Time Digital Converter

1. Introduction

The Time-of-Flight (TOF) detector of the ALICE experiment [1] has to provide particle identification information in the momentum range between 0.5 and 2.5 GeV/c in the central region through precise time measurements of pulses induced by particles crossing the MRPCs. The physics goals of such detector dictate demanding requirements (< 100 ps time resolution). In this context the choice and optimisation of the time to digital converter are critical to ensure, starting from an excellent intrinsic time resolution of the MRPC itself (≈ 25 ps) see Ref. [2], the required global time resolution.

2. The TDC readout module

The TDC Readout Module (TRM) is based on a High Performance TDC (HPTDC) ASIC [3], developed at CERN, with multi-hit and multi-event capabilities. The ASIC provides relative time measurement of each hit at external trigger arrival. It can work in four different resolution modes. When used in its Very High Resolution Mode (24.4 ps LSB), as in the TOF case, the ASIC integrates 8 channels per chip. The time digitization is based on a clock synchronous counter and a DLL interpolator. The external 40 MHz clock is internally multiplied by a PLL to feed properly the DLL to reach the required resolution. To achieve the 24.4 ps bin size, an adjustable RC delay line is used, interpolating the measurement of the same hit made by four different channels. Within the TOF context it is relevant to mention the leading and trailing edge detection capability of the HPTDC, as well as the possibility to use LVDS inputs.

The TOF readout system is described elsewhere [1]. The whole detector needs 157,248 TDC channels, with signals transmitted via 5–8 m long cable to the TRMs. The front-end electronics see Ref. [4] consists of a fast amplifier and discriminator. Output signals are shaped to provide a time over threshold (TOT) information for time slewing correction.

Fig. 1 shows a conceptual design of the TRM. The card, a VME slave card, will use 30 HPTDC chips, organised in two separate 32-bit parallel readout chains. An FPGA acts as readout controller and implements the VME interface (these two functions are separately shown in Fig. 1).

At L1 arrival, distributed to each HPTDC as trigger tag, the controller will move matched hits from the HPTDC readout FIFO to two coupled SRAM, handled by an event manager (implemented by a separate FPGA). This will mimic a dual port RAM. In this way, the readout does not need to stop when data are transferred to the internal memory of the DSP for further processing. Finally, an L2a signal will start the transfer from DSP to the output FIFO. An L2r assertion will allow the DSP to discard the relevant event. The DSP will provide online data correction (see Section 3), data packing and error tracing (notably SEU auto-detections inside internal buffers).

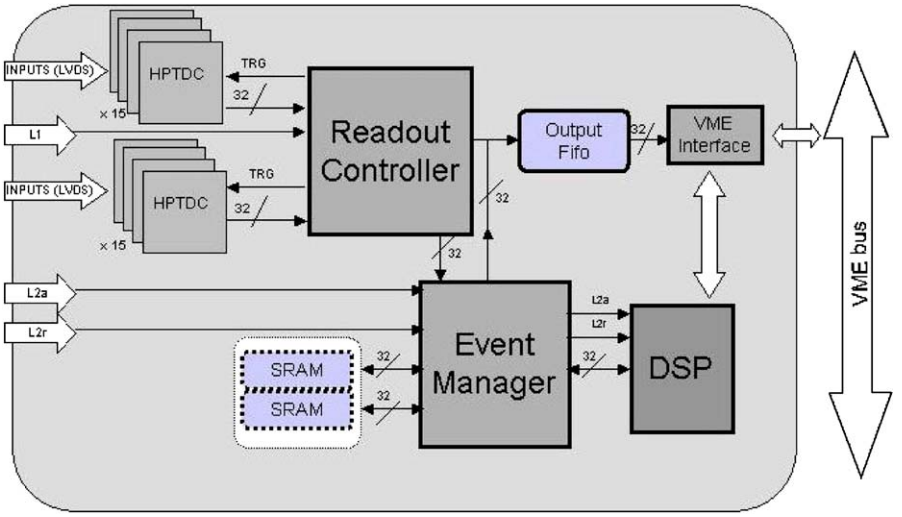

Fig. 1. TRM conceptual design.

3. Prototype cards and test results

3.1. The test cards

To test and qualify the HPTDC chips, tailor properly the proposed TRM design and develop the needed firmware, a set of prototype cards was built, separating HPTDC issues (e.g. achievable time resolution) from development of readout, data processing and trigger interface.

The HPTDC 6U slave card uses 4 chips. It is read through a private 32-bit LVDS bus implemented on P2 connector and controlled through a front-panel 20 pins control bus. A master card controls up to four HPTDC slave cards. It has on board clock, an Altera APEX FPGA, a 32-bit Sharc Analog Device DSP, two FIFOs (one to store data collected from slave cards, the other as output FIFO visible from VME) and Flash memory resources (to store DSP boot code, as well as needed look-up tables). In practice, almost all the functionalities forseen in the final TRM card were tested using these two cards.

3.2. Integral non-linearity and time resolution

In its high resolution modes the HPTDC showed a typical integral non-linearity pattern, spanning over the 25 ns cycle of the 40 MHz clock [3]. The main source of the INL was identified as coming from on-chip crosstalk from the logic part of the chip through the power supply. Despite various attempts to improve the situation at hardware level by the CERN EP/MIC group (use of a lower inductance packaging, improved distribution of the power supply) or at programming level (DLL tap adjusts can be applied), even in the last release of the chip the INL pattern is still clearly present.

The INL pattern resulted to be very stable and moderately chip-dependent. External parameters can affect it, in particular the applied core voltage, as well as the quality of the input clock feeding the DLL. We checked that in stable external conditions the pattern remains unchanged over time. To overcome the problem, the application of an INL compensation scheme through look-up tables (LUT) was a straightforward choice.

The time resolution of the device was then tested through cable length measurements, using different delay lines over the 25 ns cycle. The RMS of the measured distribution, divided by $\sqrt{2}$, is a measurement of the achievable single channel resolution. Fig. 2 shows measurements averaged over 8 pairs of channels for various delays. A resolution better than 20 ps (full circles) is reached after applying INL compensation.

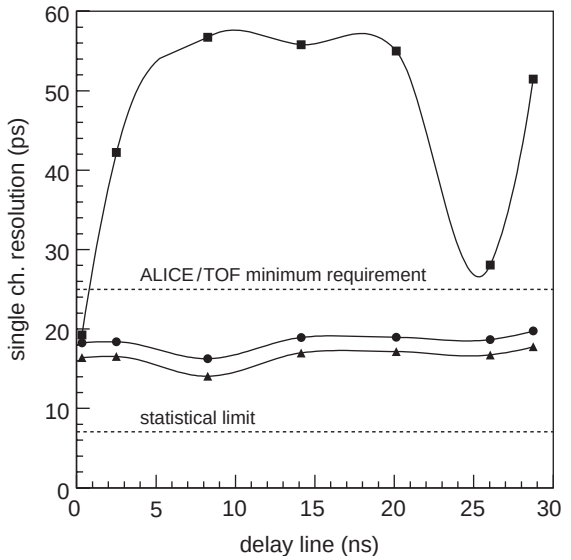

Fig. 2. Time resolution of the HPTDC for various delays: squares: without INL compensation; circles: with INL compensation; triangles: refined INL treatment.

To further improve the resolution a more refined approach was also tested. The basic idea is that, although the converter has a bin width of 24.4 ps, we know the INL pattern with a better granularity. With a small overhead it is possible to add 2-bits of information (that is use bins of 6.1 ps) to correct the INL pattern. A resolution around 15 ps for all channels was reached (Fig. 2).

The TOT signal from the front-end cards gives, with the leading edge, the time of the hit and, with the width, an equivalent measurement of the amplitude. Slewing corrections are then applied according to the measured width. In this context it was important to assess the minimum time between two consecutive measurements. The inefficiency (missing trailing edge) was found to appear very sharply just below 6 ns as expected. The front-end ASIC [4] stretches TOT pulses according to these measurements, to ensure trailing edge detection, but minimizing the dead time of the single TDC channel.

3.3. Test beam results

Since May 2002 the HPTDC prototype cards were also tested with a test beam at CERN PS, to check their performance when connected to real MRPC signals and to monitor performance stability. Initially, signals were splitted in such a way to allow comparison between measurements performed with standard electronics (LeCroy CAMAC TDCs with 50 ps bins) and with the HPTDC. The measured time resolution of the MRPCs under test was found fully compatible, confirming the time resolution of the converter estimated with the described lab benchmarks. During October 2003, the full electronic chain (front-end ASIC, LVDS transmission line and the HPTDC) was successfully tested. These results are presented elsewhere in these proceedings [2,4].

3.4. Crosstalk measurements

A major investigated concern was the shift in the measured time difference between two signals, generated at the ASIC level by crosstalk from another firing channel. We measured a fixed time difference (obtained by means of a delay line) between two signals, digitising them in two separate chips. A noise signal was then injected in the other channels of the chip measuring the start signal, at various time distances from it. All the signals used had 10 ns width, with leading and trailing edge detection enabled. At the 20 ps level it is really difficult to build a "noise free" set-up for this kind of measurement. To isolate the contribution of the chip, two sets of measurement (shown in Fig. 3) enabling and disabling by software the noisy channel were done. Even if a small perturbation is present when the HPTDC channel receiving the noise signal is enabled (when the time from noise to signal is between –10 and 0 ns), the effect has been satisfactorily checked to be within 1 LSB over all tested channels.

In MRPCs there is a distinct probability to observe signals in two neighbouring pads when a particle hits the pad boundary, due to a charge sharing effect. At the same time near the boundary, due to a smaller collected charge, the resolution is normally worse [1]. By means of a beam scan of two neighbouring pads, we checked that the HPTDC does not introduce an additional contribution to this effect due to crosstalk.

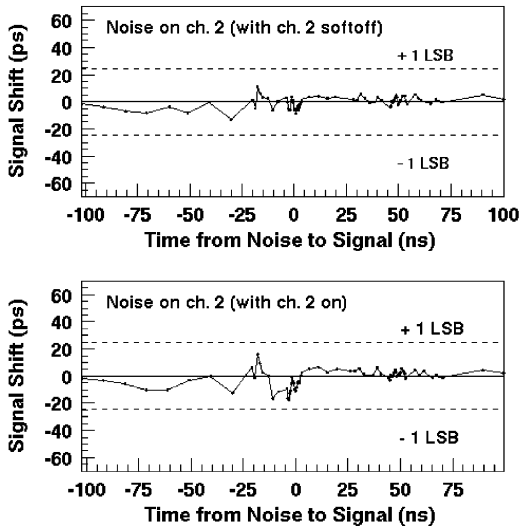

Fig. 3. Signal time shifts measured as a function of the distance of the signal in another HPTDC channel.

4. Conclusions and outlook

Having tested functionalities and performances of the HPTDC, we are now planning the final layout of the 240 channels card. Additional tests, not discussed in this paper, are also under way, such as operation inside a magnetic field and radiation tolerance. Taking into account the front-end modularity and the need to reduce the card complexity, 10 piggy-back cards plugged on both sides, each using 3 HPTDC and local voltage regulator, are foreseen. Besides FPGA and DSP, the central main board will be equipped with Flash RAM for look-up tables and firmware (upgradable via VME), latch-up protection systems as well redundancy and watchdog mechanisms to react properly to SEU events.

The HPTDC has been thoroughly tested and qualified in its Very High Resolution Mode for ALICE TOF. It was shown that, after applying INL correction, a conservative 20 ps resolution is achieved. The building "bricks" of the final TRM card have been tested as well as its key functionalities.

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