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Generic foundry model for InP-based photonics

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Abstract: Similarities and differences between photonic and microelectronic integration technology are discussed and a vision of the development of InP-based photonic integration in the coming decade is given.

1 Photonic integration: introduction

After its emergence at the end of the 60s [1], it was believed that photonic integration would take a similar development path to that followed by microelectronic integration. In his review paper in 1977, Tien [2] mentioned as one of the major goals of photonic integration or 'integrated optics' as it was called at the time: 'the integration of a large number of optical devices on a small substrate, so forming an optical circuit reminiscent of the integrated circuit in microelectronics'. In the following years, a number of chips with increasing complexity were reported [3–7]. However, despite large R&D investments, photonic integrated circuits (PICs) with integration levels exceeding a few components did not succeed in entering the commercial marketplace for more than four decades. Sceptics started claiming that integrated optics was a promising technology and would ever remain so. It took until 2005 before the company Infinera introduced the first truly complex PIC in a commercial wavelength division multiplexing (WDM) system: a 10-channel WDM transmitter with more than 50 components integrated on a single InP chip, with a total capacity of 100 Gb/s [8]. Until now this is the only PIC of such a complexity that has been introduced commercially, although recent developments in the field of advanced modulation formats for telecommunications systems (like diquadrature phase-shift keying (DQPSK), pulse modulation DQPSK and quadrature amplitude modulation) indicate that other highly complex PICs will follow soon [9–12].

It is an interesting question to ask why so few of the advanced PICs reported in the literature have made it to the commercial arena up until now, despite the fact that over the last two decades there has been substantial investment and improvement in the development of integration technologies in industrial, national and international projects in Europe, in America and in the Far East.

An important factor delaying the breakthrough of photonic integration to commercial applications has been the shift in technology focus from 'technology push' to 'market pull', which occurred in the early 90s of the last century. It became increasingly difficult to obtain funding without a clear and challenging system application. Viewed in isolation this seems to be a good policy for preventing the development of technology for which there is no market, as had happened frequently in the more distant past. But it had some important and undesirable side-effects which hampered the breakthrough of photonic integration. In most of the application-oriented projects, the coordination was done at the system level, and at the device level each technology partner was responsible for his own device. There was an almost complete lack of coordination in technology development, every fab developed its own processes and there was no incentive for process standardisation. As a result, we have almost as many technologies as applications, most of them very similar in their objectives, but sufficiently different to prevent both easy transfer of a design from one fab to another, and easy use of the technology for applications other than the ones for which it was developed. Owing to this huge fragmentation, the market for these application-specific technologies is in most cases too small to justify their further development into a low-cost industrial volume manufacturing process. Consequently, the chip costs remain too high to serve a large market and commercial use of PICs is limited to specific applications where they bring unique functionality that is not available in other technologies.

To overcome this fragmentation, the way forward is to develop a small set of standardised technologies, in which the most frequently used basic building blocks are brought together in a single integration process, which is optimised for providing high performance for all the building blocks: a fabrication platform. Such a standardisation effort requires substantial investments in technology development, for which there was no budget available in the industrial development programs, because the market for their specific applications was too small, and

also not in government-funded research programs, because these became increasingly application-oriented since the 90s.

Another barrier was a general belief that photonics is so different from electronics that it is not possible to construct a generic technology without compromising performance in an unacceptable way. This belief was not only shared by policy makers, program leaders and reviewers, but by many people in the research community itself, and as a result there were few attempts to move in this direction.

This is quite different from the situation in micro-electronics, where a huge market is served by a relatively small set of integration technologies (most of them complementary metal–oxide semiconductor (CMOS) technologies). The solution to this problem in photonics seems obvious: apply the methodology that allowed microelectronics to change our world to photonic integration as well. This requires two steps:

- Develop a few generic integration technologies that support realisation of a broad range of functionalities.
- Develop a foundry infrastructure for providing low-cost open access to these generic technologies.

After the telecom bust shortly after the beginning of the century, it became evident that the huge fragmentation of the technology landscape was no longer sustainable and discussions about a foundry model for photonics and foundry technology development began to appear on the agenda of policy makers. This required a shift to a more balanced mix of 'market pull' and 'technology push' funding policies, however, and it was only recently that the first large-scale projects aiming at generic technology development could be started.

2 Generic photonic integration technology

In micro-electronics a broad range of functionalities is realised from a rather small set of basic building blocks, like transistors, diodes, resistors, capacitors and interconnection tracks. By connecting these building blocks in different numbers and topologies, we can realise a huge variety of circuits and systems, with complexities ranging from a few hundred up to over a billion transistors.

In photonics we can do something similar. On inspection of the functionality of a variety of optical circuits, we see that most of them consist of a rather small set of components: lasers, optical amplifiers, modulators, detectors and passive components like couplers, filters and (de)multiplexers. By proper design these components can be reduced to an even smaller set of basic building blocks.

As basic building blocks we need passive devices for combining and splitting of light, both wavelength-dependent (filters, wavelength multiplexers) and wavelength-independent (power splitters, couplers and combiners). Most of these devices can be composed of a combination of passive waveguides of different widths and lengths. So in a proper integration process that supports integration of passive waveguides, a variety of passive devices, such as multi-mode interference (MMI) couplers and arrayed waveguide gratings (AWGs) can be realised. In addition to these passive devices, we need basic building blocks for manipulating the phase, the amplitude and the polarisation of the light signal, in order to support a broad range of functionality.

Fig. 1 illustrates some functionalities that can be realised in a generic indium-phosphide technology that supports integration of four basic building blocks: passive waveguide devices, phase modulators, semiconductor optical amplifiers and polarisation converters. Many of the functionalities shown in Fig. 1 have been reported by COBRA: compact MMI-couplers [13] and AWGs [14], optical switches [15] and modulators [16], multi-wavelength and tunable lasers [17], flip-flops and ultrafast wavelength converters [18], picoseconds pulse lasers [19] and polarisation splitters and converters [20]. Fig. 2 shows an example of an integrated tunable laser with nanosecond switching speed [17], useful

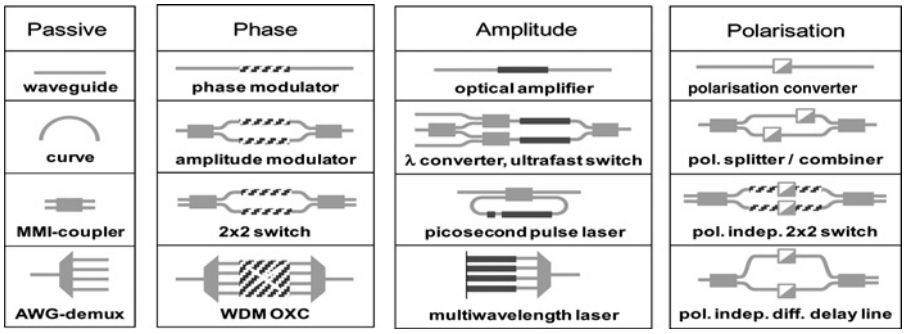

Fig. 1 *Example of the functionalities that can be realised in a generic integration technology that supports four basic building blocks: passive waveguide devices, (optical) phase modulators, semiconductor optical amplifiers and polarisation converters*

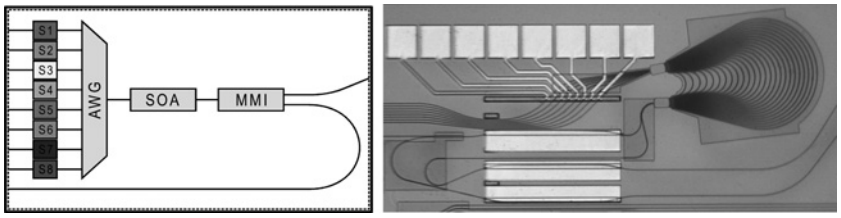

Fig. 2 *Circuit scheme and microscope photograph of an AWG-based fast tunable laser, which has been realised in the COBRA InP-based generic integration process*

Chip dimension is 1.5 × 3.5 mm^2

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for packet switching applications, which has been developed in our experimental generic integration technology. The schematic on the left shows how the laser is composed of only two basic building blocks: passive waveguides in the MMI-coupler, the AWG demultiplexer and the interconnections and semiconductor optical amplifiers for amplification and switching.

Because generic integration technologies can serve a large market, they justify the investments in developing the technology for a very high performance at the level of the basic building blocks, which will make circuits realised in this technology highly competitive. Of course, a single platform will not yield equally high performance for every conceivable application. Just like in microelectronics different classes of applications need different processes, for example, high voltage, high speed, high power or low power, and so on. In a similar way, photonics will need a few different generic technologies, optimised for different classes of applications, to cover a major part of all uses. But the number of generic technologies required is far smaller than the number of technologies which are presently in use.

3 Generic foundry model in photonics

Once a mature generic integration technology has been developed, it needs to be made accessible with a low entry barrier to a large number of users. In microelectronics, programs like MOSIS [21, 22] in the US and EUROPRACTICE [23] in Europe organise low-cost access for universities and companies by bringing designs from different users together in so-called multi-project wafer (MPW) runs. In this way they transform a number of smaller customers into a bigger one with sufficient volume to get access to the foundry. After fabrication the wafers are diced and each customer gets his own chips. In this way the low-chip costs that are realised for large volumes in standardised foundry processes also become available to smaller users. In photonics the first steps in this direction are now being taken.

3.1 Custom foundry model

After the turn of the century, forced by the high exploitation costs and the small load of their clean rooms, a number of photonic fab owners opened their fabs to external, so called fabless users. These companies, which call themselves foundries, develop processes for specific customer components and requirements, in close cooperation with the customer. Usually the process is owned by the customer, who paid for its development. This approach led to a significant reduction of the entry costs for newcomers, because they do not have to build their own clean room, but share the costs of the cleanroom with a large number of other fab users. In this model the process development is still application-specific; however, the associated costs will not be shared with other users. We call such a foundry, therefore, a custom foundry, and the approach the 'custom foundry model'. Because the process development costs are not shared, the entry costs remain significantly higher than in microelectronics, where existing generic foundry processes are available for the development of application-specific ICs (ASICs), so that not only the cleanroom costs, but also the process development costs are shared by a large number of users.

3.2 ePIXnet

In photonics, generic foundries are non-existent today, but the first steps towards their creation were made by the FP6 Network of Excellence ePIXnet (European network of excellence on photonic integrated components and circuits). It was started in September 2004 with a large number of academic and industrial members on an ambitious mission: to move from a model of independent research to a model of integrated research with shared use of expensive technological infrastructure. In the background were the steadily increasing costs of clean room facilities that restricted photonic integration research to the ever smaller group of institutes that could afford a clean room. The idea was to enlarge the group of users by stimulating clean room owners to organise access to their facilities for a broader circle of non-clean room owning partners. After experimenting for two years with facility access activities, the ePIXnet Steering Committee published a vision document [24] about a foundry model in micro- and nanophotonics. Integration technology platforms for offering open access to a few major integration technologies were set up in ePIXnet in that same year.

3.3 ePIXnet integration technology platforms

Two major integration technologies were identified: InP-based integration technology, which supports the highest degree of functionality, including compact lasers and amplifiers, and silicon photonics technology, which offers most of the functionality offered by InP except for the compact lasers and amplifiers, with good process uniformity and low cost because of its compatibility with mature CMOS technology, operating on large wafer sizes. For both technologies, a platform organisation was established; JePPIX for InP-based integration technology [25] and ePIXfab for silicon photonics [26]. Later a third platform with dielectric waveguide technology was added, which offers low-loss and high-quality passive optical functions and some thermo-optic active functions, through the whole wavelength range from visible to infrared (TriPleX, [27]). All the three platforms started by providing open access to a relatively mature integration technology for research purposes: the JePPIX platform to the InP-based integration technology of the COBRA Research Institute of TU Eindhoven, the ePIXfab platform to the SOI-technology of IMEC and the TriPleX platform to the TriPleX technology of the Dutch company Lionix.

3.4 MPW runs

All the three platforms offer access to their technologies through MPW runs, a well-known concept in micro-electronics, but not previously applied in photonics. MPWs lead to a significant reduction of the costs of chip R&D by combining designs from different users in a single wafer run, so that the costs of a run are shared. Fig. 3 illustrates how this is done. The figure at the left shows how a sample is subdivided into nine sectors, three for testing and six for user designs. The picture in the middle shows an actual mask design from a JePPIX MPW run in the COBRA process and the picture at the right a photograph of the realised chip (before cleaving of the individual user chips and test chips). On a 3′ wafer such a pattern can be repeated more than 10 times. In a process batch with three 3″ wafers each user would have more than 30 copies of his

Fig. 3 *Example of a MPW realised in the COBRA process*

The wafer is subdivided into nine sectors, three for test structures and six for user designs. The picture in the middle is an example of a mask layout, and at the right is a photograph of the realised chip

chip, which is usually more than sufficient for testing the design and coming to a redesign, if necessary.

3.5 Generic foundry model

The initiatives taken by ePIXnet were first steps towards full introduction of the generic foundry model in photonics. In a fully operational model, the following activities have to be addressed:

1. Access to mature and well-documented industrial foundry processes via full or MPW runs.
2. Availability of dedicated design software and component libraries, calibrated against the platform capability, enabling fast and accurate design (design kits).
3. Training and support of users not familiar with the technology.
4. Brokering service for assembling different user designs into a mask set for a MPW-run.
5. Specialist design houses which can help users who do not have the know-how to design their own chips.
6. Access to generic test facilities.
7. Access to generic packaging facilities.

This model is well known in microelectronics for the development and manufacturing of ASICs. The ePIXnet integration technology platforms are presently gaining experience with all these activities at a research level and a number of projects have been started to explore the generic platform approach in depth, in an industrial environment and with designs contributed by third parties. In this way we are introducing the concept of ASICs in photonics, where we will call them ASPICs: application-specific photonic ICs.

4 Prospects for generic photonic integration

4.1 R&D time and cost reduction

Adoption of a generic foundry model could lead to a dramatic reduction in the costs of PIC R&D and manufacturing for small or medium volumes, and to a significant reduction of the number of R&D cycles needed to arrive at a properly functioning prototype. Below we will discuss the magnitude of the anticipated cost reduction. The numbers are only indicative and may strongly differ from case to case, depending on chip size and complexity, and production volume.

The chip costs are made up of two components, an R&D component and a manufacturing component. A third important component is the cost of packaging. The R&D costs consist of the cost of process development, chip design, the test runs required for arriving at the required specs and the cost of qualification and package development.

4.1.1 Manufacturing costs: The manufacturing costs of a chip consist of the depreciation and the exploitation costs of the fab, divided by the total number of chips or, more accurately, the chip area produced in a year, and the cost of materials. The depreciation costs per chip get lower the better the fab is loaded. With a reasonable fab load they can be of the order of a few Euros per mm^2. For comparison, the cost of CMOS silicon is of the order of a few cents per mm^2, that is, two orders lower. With further development and scaling of the photonics technology, the difference may be reduced to less than a factor of ten. Material costs (substrates, gases etc.) are usually only a small part of the total chip costs, which tend to be much more dependent on the total number of process steps than on the specific materials used. For large chip volumes the cost advantage of generic manufacturing over custom manufacturing will get smaller, but for small volumes it can be significant through the use of MPW runs, where the costs of a full run, containing thousands of chips, can be shared by a number of different ASPICs.

4.1.2 Cost of process development: The costs of developing a novel process in a custom foundry, including PIC qualification tests, are in the order of one up to many million Euros, dependent on the complexity of the chip, the process and the background knowledge of the foundry. In a generic approach there are no additional process development costs, because all ASPICs use the same existing process. Even though the initial process development costs are higher because of the high functionality and performance requirements, in a generic foundry approach their contribution to the total chip costs will be smaller by several orders for smaller volumes. For larger volumes the advantage gets smaller, because in the custom foundry approach the costs can be distributed over more chips.

4.1.3 Cost of prototype development: The costs of a single run in a mature process are smaller by one or two orders of magnitude than the costs of developing the process. So even if a few runs are required to arrive at a satisfactory prototype, the fab cost reduction in using a mature foundry process may be in the order of a factor of 10.

4.1.4 Qualification cost: A significant part of the cost reduction of generic manufacturing is in testing and qualification of the chip, which is a major cost factor for

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chips for which reliable operation is required over long periods of time and under harsh conditions. Most of the qualification applies to the manufacturing and packaging process and this part need not be repeated for each individual product; it applies to all PICs that are developed according to the design rules. Generic manufacturing may bring a major cost reduction also here.

4.1.5 Design costs: Through the availability of accurate, dedicated design software, the number of R&D cycles needed for getting a chip into specification will be greatly reduced. And a major advantage of the use of generic foundry processes is that they support building of powerful component and circuit libraries, in which a variety of tested and accurately specified components and circuits are available to the designer with a few mouse clicks, which would otherwise have taken him or her months of design work. This will not only lead to a reduction of design time and a smaller number of test runs for arriving at a properly functioning prototype, but it will also allow for successful design of PICs with a much larger complexity. For complex chips the availability of a powerful design kit including an extensive component library may easily reduce design times from years to months, or from several months to a few weeks, for less complex designs. This is again a cost reduction of an order of magnitude, in combination with a strong reduction of the time-to-market.

4.1.6 Packaging costs: A major contribution to the total costs of a component or module are the packaging costs, for simple components they are several times higher than the chip costs, and even for complex chips they will be the dominant cost factor. For the generic foundry approach to become successful, therefore, the large reduction in chip costs should be accompanied by a similar reduction in packaging costs. This should be achieved by introducing a large degree of standardisation in positioning of electrical and optical input and output ports and by development of automated generic packaging technologies that can be applied to a variety of different chips which have the same form factor.

Fig. 4 illustrates the cost reduction mechanisms discussed above for three different manufacturing models in a strongly simplified calculation in which the chip costs are represented as the sum of the entry costs divided by the total produced chip volume (using the measure of chip area in mm^2) and the marginal chip costs. The latter have been assumed to be the same in the three models and set to a fairly arbitrary 3 €/mm^2 in the figure.

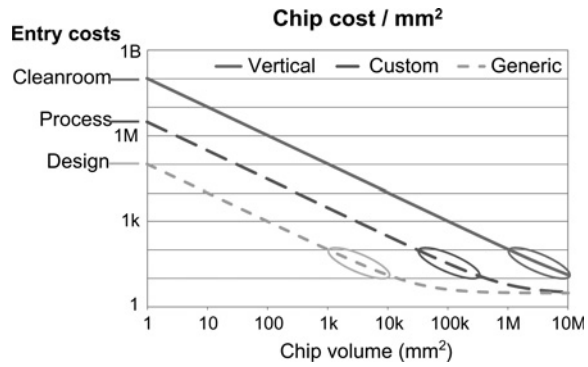

Fig. 4 *Illustration of the dependence of chip cost (per mm^2) on the total chip volume (in mm^2) for three different manufacturing models*

The entry costs are strongly different: for a vertically integrated fab, where the chip supplier owns the clean room and the process, they can be as high as a few hundred million Euros for a top-class clean room. With such an investment a total chip volume of more than 1 million mm^2 is required to bring the entry costs per chip under 100 €/mm^2, as indicated by the ellipse in Fig. 4. This is equivalent to just 250 processed 3′ wafers; a large InP fab would be capable of processing many times this number of wafers in a year.

In the custom foundry model, the entry costs are dominated by the process development costs which may, including qualification costs, be as high as a few million Euros. In that case the required chip volume to get the entry-costs per chip under 100 €/mm^2 is in the order of 100 000 mm^2. This is only true, of course, if the total volume of all wafer runs by the foundry is sufficiently large to reduce the costs of clean room amortisation per chip to a small fraction of the actual chip cost.

In the generic foundry model, the entry costs are dominated by the design costs, which in principle can be in the order of 100 k€ or even less. In this case chip volumes between 1000 and 10 000 mm^2 are already sufficient to bring the entry costs below 100 €/mm^2. Once again we assume here that the costs of clean room amortisation and process development on a per chip basis are small in comparison to the actual chip costs. This will happen if sufficient users share the same generic process.

At this point we want to stress again that these numbers are only indicative and can differ significantly from real numbers in individual cases, depending on process and chip complexity. We use them only to provide some quantitative feeling for the cost advantages that can be realised in the different models. However, the figure reflects the general features expected from the different cost models with the costs per mm^2 converging on the base cost at the highest volumes. A clear conclusion from the figure is that the generic foundry model is particularly attractive for smaller volumes, where it may reduce chip costs with more than an order of magnitude.

A conclusion, valid for all three models, is that the advantage of integration increases with increasing circuit complexity because it avoids the costs of packaging all individual components. As long as packaging costs are dominant, the additional complexity integrated in a PIC comes almost for free. But to become competitive with other technologies also for lower PIC complexities, it is important that the packaging costs are strongly reduced by developing generic packages and packaging technologies. Another advantage of the generic foundry model is that once a prototype has been developed, the road to manufacturing is short: the same process supports fabrication of both small and large numbers of chips.

4.2 Intellectual property (IP) in a foundry model

In a custom foundry model, handling IP of the design and the process can be fairly complicated, because the IP is generated in a close cooperation between the foundry and the user. In a generic foundry model the separation of IP between foundry and user is much clearer because chip design and process development are strongly decoupled. The foundry process is developed and owned by the foundry. The chip design is owned by the designer, who does not need to inform the foundry about the chips that he is fabricating in the foundry: the foundry is application-blind. It does a design-rule check on the designs that are offered, but in the end

this should be fully automated, so that the foundry does not get any specific information about the user designs. This implies that the user owns all IP of his own design, and can also be made fully responsible for any violation of existing IP in his design.

4.3 Market development

The anticipated large reduction of R&D time and chip manufacturing costs should lead to a large growth of the share of PICs in the photonic components market. So far the use of PICs has been mainly restricted to specific areas in telecom core-network applications, where their specific functionality cannot be met by competing technologies. With the expected cost reductions through a generic foundry approach, they will also become competitive in high volume markets like the telecom access network, where they may be applied in the Central Office for integration of larger numbers of circuits that have to be repeated for each subscriber or group of subscribers. In future 10 Gb/s access networks may also become competitive in the subscriber transceiver module.

When R&D and manufacturing costs drop, photonic chips will increasingly penetrate into other applications. A good example is the fibre sensor market, which was over 400 M$ in 2008 with double digit annual growth figures. According to a recent GIO report, it will exceed 2 B$ in 2015. A significant part of the sensor costs is in the readout unit, which contains one or more light sources, detectors and some signal processing circuitry. Here PICs can replace a significant part of the existing modules and enable novel sensor principles to be exploited. Examples are various types of strain sensors, heat sensors and a variety of chemical sensors [28].

Optical coherence tomography (OCT) is another potential application. Traditionally OCT is done in the 800 nm window, which is the preferred choice for retina diagnostics. For skin or blood vessel diagnostics wavelengths longer than 1500 nm are better, because there the penetration depth is three times as large due to reduced scattering losses at this wavelength. This provides good opportunities for InP PICs in OCT equipment [29].

Another interesting class of devices comprises pico and femtosecond pulse lasers [30]. Here PICs containing mode-locked lasers, optionally combined with pulse shapers, can provide small and cheap devices that can be used in widely differing applications, such as high-speed pulse generators and clock recovery circuits, ultrafast A/D-converters and in multi-photon microscopy.

These are just a few examples. Once ASPICs get to be really cheap, they will offer ample opportunity for small and large companies to improve their competitiveness by applying them in their products.

5 Discussion

In this section, we will discuss a number of aspects of generic integration and the foundry model which are frequently raised.

5.1 Compromised performance?

A frequently heard objection to the foundry approach is that it will not be possible to provide a broad functionality in a standard process without compromising performance. We believe that in an approach in which a broad class of functionalities is realised from a small set of basic building blocks, it will be possible to optimise the generic process for record performance of the basic building blocks. By proper design this can be translated into record performance of more complex circuitry in many cases. By concentrating investments in a small set of standardised technologies, the performance and capabilities of these technologies will steadily increase and outperform more and more application-specific technologies. Such a development has been observed in silicon microelectronics, which in the past decades has outperformed many potentially superior technologies, just because of the much higher investments made in silicon technology.

We expect a similar development in InP-based generic integration technology. In the EU-FP7 project EuroPIC [31], 17 European partners are cooperating in exploration of the potential of the generic platform approach, utilising the integration technologies of Oclaro and the FhG Heinrich Hertz Institute (HHI) and setting up a basic design environment needed to facilitate the operation of a generic foundry. The platforms developed in this project are based on the high-performance processes in which Oclaro fabricates its tunable lasers and high-speed modulators and in which HHI fabricates its high-speed receivers. In the project PARADIGM [32], several of the same organisations, along with some additional partners with complementary expertise, are exploring the feasibility of a next generation foundry technology with additional capabilities and performance: transmit and receive functionality up to 40 GHz, free choice of material band gap through the C-band, inclusion of buried heterostructure (BH)-SOAs and lasers. Further, the project addresses development of powerful design kits and component libraries and a low-cost generic packaging technology. If these projects are able to demonstrate the technical feasibility of the generic foundry approach and the way forward is set for the additional investments that will be needed by the wafer fabs in order to convert this opportunity into a new business model, first commercial operations could commence in the second half of the present decade.

5.2 Photonics too different from microelectronics to apply the same methodology?

Too many different components and technologies, wavelength ranges, and so on? Since we started developing the generic foundry philosophy in the ePIXnet network of excellence, we have become convinced that the difference in approach between the photonics and the microelectronics community is restricting progress in the former group. Discussion with microelectronics pioneers has taught us that microelectronics has gone through a similar transformation from application-specific technologies to generic technologies during the 1980s and that many of the present objections against generic photonic integration were also heard during that period of development in the electronics world. Our experience in foundry-based research projects like EuroPIC and PARADIGM is that many of the concepts used in microelectronics, like MPW-runs, component libraries and so on, can be applied with great advantage in photonics too.

5.3 Competition with silicon-photonics?

Another point of discussion is whether there is a sufficient outlook for an InP-based foundry technology, in view of

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the promise of silicon photonics to offer photonic technology in a CMOS environment offering advantages of scale. We are convinced of the potential of silicon photonics for development and fabrication of circuits which are not critically dependent on lasers, optical amplifiers or high performance modulators. Integration of efficient lasers and optical amplifiers in silicon is as yet an unsolved problem, although a number of exciting solutions are being explored. Most of them require special technology, for example, hybrid integration of III–V materials, which strongly reduces their CMOS compatibility. A number of problems have still to be solved, such as low-cost packaging, and the balance between hybrid and monolithic approaches, which are not so much different for silicon and InP-based technology. We expect, therefore, that in the short-term InP-based generic integration will offer better potential for more complex circuitry that requires the integration of lasers and amplifiers. One can speculate that in the longer term both technologies may converge into a technology in which the photonic functionality is provided by a thin InP-based membrane on a silicon or CMOS substrate [33].

5.4 Monolithic or hybrid integration?

For a long time there have been discussions whether hybrid integration of active InP components in a PLC-like silicon motherboard could provide a better solution than monolithic integration alone. We think that monolithic and hybrid dielectric waveguide technologies are highly complementary: complex monolithic chips, especially those with multiple densely spaced output ports, require dielectric waveguide chips to connect them to the fibre world. In the EuroPIC and the PARADIGM projects, we are working on the development of a generic packaging approach based on a standardised silicon motherboard, in which complex monolithic InP-chips with standardised positions for the optical and electrical ports are mounted. Such an approach may provide us with a hybrid platform in which the best of both technologies can be combined and in which more and more functionality can be integrated when the performance and the capabilities of the monolithic integration technology increase.

5.5 Research in a foundry model

Some academic researchers fear that the standardisation that forms the basis of the foundry approach will restrict the room for research. We expect that the opposite will happen. When generic integration technology becomes the dominant manufacturing model, large investments will be made in the development of novel generations of technology with an ever-increasing performance and functionality, in a similar fashion to microelectronics, where every few years a novel technology generation (node) is launched. This development generates a large demand for physics research into technology and equipment, in order to push the technology to the fundamental limits, and invent new approaches in order to overcome the present limits. And finally, just like in microelectronics, the foundry approach will create a new field of science in design of circuits with an ever-increasing complexity and functionality up to a level that will go beyond our present dreams.

6 Conclusions

By applying the methodology of microelectronics to photonics, we expect a dramatic reduction of the costs for R&D and manufacturing of PICs and a breakthrough to a wide range of application fields, not only in telecommunications and data communications, but also for application in sensors, medical equipment, metrology and consumer photonics. Such a breakthrough will accelerate the development of more advanced integration technologies.

Owing to their much lower costs and shorter development time, we expect that the market for ASPICs realised in generic foundries will grow much faster than today's PIC market, so that the generic foundry approach could become the dominant model in photonics well before 2020.

InP-based technology and silicon photonics are promising technologies for generic foundry platforms offering a very high functionality. Interesting opportunities also exist for dielectric waveguide technologies, like the TriPleX platform. In the longer term InP and silicon technology may converge into a technology that combines the best of both.

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