Hardware for the Detector Control System
of the ALICE TRD
(Stand-alone embedded Linux controller)

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Abstract

The presented DCS single board computer represents the front-end of the detector control system of several detectors in Alice including TRD and TPC. The device is equipped with Alteras's Excalibur FPGA, comprising of both a 100 k gate FPGA and an embedded ARM processor on which the operating system Linux is running. The FPGA is used to customize the device for different front-end environments. Communication with the board is based on Ethernet which is modified in order to operate in magnetic fields. Since the board has to operate under radiation conditions special care has been taken during the design process to ensure high reliability.

I. INTRODUCTION

ALICE (A Large Ion Collider Experiment) [1] is an experiment optimized for the study of heavy ion collisions at a center-of-mass energy per nucleon pair of 5.5 TeV. The central detectors – comprising an inner tracking system (ITS), a large time projection chamber (TPC), a time-of-flight array (TOF), and the transition radiation detector (TRD) – cover the range $-0.9 \leq \eta \leq 0.9$ in pseudo rapidity with complete azimuthal coverage. The main task of the TRD [2] is the identification and trigger of electrons with transverse momenta exceeding 1 GeV/c. The detector consists of 6 individual layers and is segmented into 18 sectors in azimuthal direction. In total there are 540 detector modules, covering a total area of 767 m^2 and a gas volume of 28 m^3. The detector raw data are read out with about 1.2 million independent channels comprising a preamplifier, an ADC, and a digital chip for online data processing.

Detectors of such a complexity require a sophisticated control system for monitoring and control of the overall working conditions like voltages, temperatures, and pressures. This system has to be able to react to critical situations in order to avoid damages to the detector. In addition, the front end electronic has to be initialized and configured depending on the actual running conditions which include e.g. downloading pedestal values to the front end electronic. This entire functionality is performed by the experiments' Detector Control System (DCS). This system consists of a number of hardware and software components on three hierarchical layers. Supervision and control of the different detectors take place on the first layer, the supervision layer. Besides others, this layer covers man-machine interfaces and configuration databases. In addition, application programs operating the detectors are running on this layer. On the control layer the collection and processing of data takes place. The last layer, the field layer, is dedicated to the connection of the detector equipment via sensors, I/O-interfaces, and field buses to the DCS.
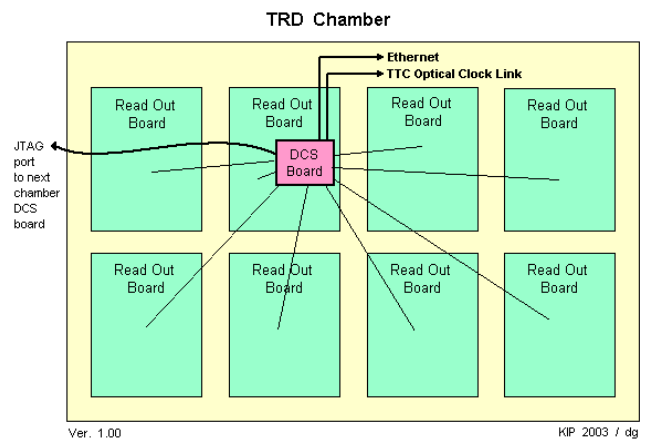

Figure 1: One DCS single board computer monitors and controls the eight read-out boards of one TRD chamber.

The front-end of the TRD detector control system is the DCS single board computer, a small autonomous single board Linux computer, detailed in this document. One DCS single board computer is responsible for monitoring and controlling the eight read-out boards of one TRD chamber and the front end electronic attached to it (see Figure 1).

II. THE DCS-SINGLE BOARD COMPUTER

A. Embedded System

Due to the manifold tasks of the DCS single board computer a flexible system is needed which can be easily adapted to changing requirements on the field layer of the detector control system. Such complex systems are usually

realized with embedded microcontrollers which excite specific application software. However, such systems often use highly specialized controllers and require a large effort during the software design process since the microcontroller are often programmed in assembler code or require specific software environments and host computers to interface to. On the DCS single board computer Alteras' Excalibur FPGA with embedded ARM core is used. The ARM processor runs Linux as operating system, therefore simplifying the development of application software. All Linux standard tools for software development can be used on any Linux computer. Most of the software, except for the hardware interfaces themselves, can even be tested on any Linux computer. In addition, the integrated, programmable FPGA allows the integration of specific functionality in a very flexible way and is being used to custom fit the device to the specific requirements of the detectors. For instance, it hosts the TRD slow control serial network interface (SCSN) for maintenance of the various front-end modules. In case of the TPC the FPGA hosts the interface to the front-end controllers, which maintain the TPC readout chips.
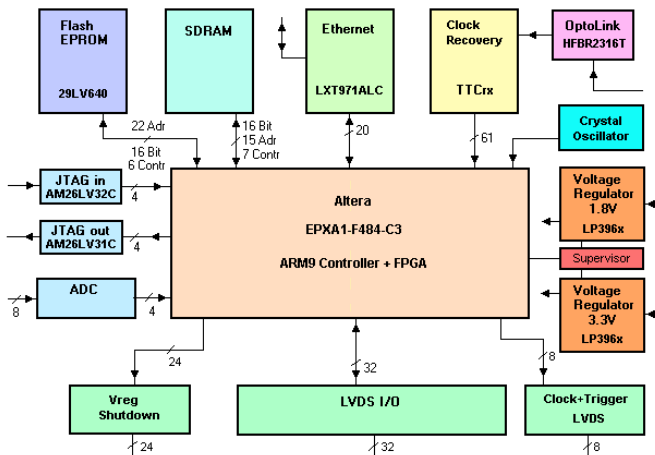

Figure 2: Block diagram of the DCS single board computer.

Figure 2 shows a block diagram of the DCS single board computer. The central component is Alteras' Excalibur FPGA. The FPGA configuration and the CPUs program code is stored in a Flash ROM from which the system is automatically configured after power-up.

For the purpose of monitoring critical parameters like temperature or supply voltages, the DCS single board computer has inputs for analog signals which are digitized by an on-board 16-bit ADC. Control lines running from the board to the front end electronics voltage regulators make it possible to switch the entire electronics off. The DCS single board computer is operating on an autonomous power supply. Supplementary bidirectional and in part differential connections between the detector and DCS single board computer can be used for the integration of additional control tasks or the adaptation of the existing hardware to new detectors. Another task of the DCS single board computer is the distribution of the global clock and trigger information to the front end electronics on the detector. This information is delivered to the board via an optical link and distributed with

LVDS connections. A SDRAM chip and a physical layer chip for Ethernet connections complete the system.
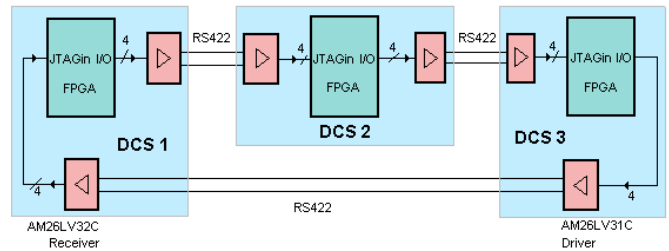

Figure 3: JTAG reconfiguration scheme.

Since the DCS single board computer has to operate in a harsh environment with radiation exposure and is very difficult to access, special care has been taken on the design of the board in order to ensure high level of reliability and maintenance features. Full control over all on-board configurable components, such as the FLASH memory or the FPGA, is ensured and reconfiguration of these components during detector operation has been foreseen. For instance, all boards on the TRD are connected in a ring structure. Each board implements a JTAG master which can be used to fully reconfigure the next board downstream. All signals are fully differential in order to avoid any ground loop issues. Figure 3 shows a sketch of the resulting JTAG reconfiguration ring structure. Basically all single board computers can be debugged and reconfigured using JTAG, provided that at least one device remains operational and no severe hardware damage exists.

B. Software

The DCS single board computer runs ARM-Linux as operating system, a version of the Linux operating system. This simplifies dramatically the development and adoption of software since the well known GNU standard tools (compiler, debugger, and libraries) can be used. Using a cross compiler for ARM CPUs allows comfortable development of software on each PC running a standard distribution of Linux. During the development process the executable binaries can be stored on external discs which are mounted via NFS to the DCS single board computer. This approach eliminates the need for time consuming downloads of the software to the Flash ROM during the software development phase. Typically only the fully debugged version is transferred for non volatile storage to the Flash ROM. Booting the Linux kernel is done by *ARMboot* [3], an open-source project suited for embedded systems based on ARM CPUs. The program is easily portable and can be adapted to different hardware configurations like the DCS single board computer operating the TRD or TPC.

The usage of a cross compiler allows the utilization of a wide variety of existing user applications on the DCS single board computer. For instance, a web server was successfully ported and operated on the board. This allows for a very comfortable configuration and monitoring scheme of individual detectors based on the http protocol together with

the common gateway interface (CGI). Any web browser in combination with the on-board web server can be used as an interface to the detector and allows for the execution of commands (e.g. configuration of front end electronic or power on/off) or the display of detector parameters like temperature, pressure, or supply voltages. The high level control and monitoring functionality of the detector control system is based on the *Distributed Information Management System* (DIM) [4]. This requires a so-called DIM-server running on the DCS single board computer. This server is responsible for publishing measured slow-control data to the next higher instances in the hierarchical DCS system. Commands to the DCS single board computer are also sent to the server. An appropriate DIM server was ported and is operational on the first prototypes of the device.

Booting the DCS single board computer to date requires less than 10 s. There is room for further speed-up. The boot sequence includes configuration of the FPGA, initialization of the ARM processor, and start of the Linux kernel. All programs necessary for the starting the system and its operation are permanently stored on the Flash ROM. Therefore, the DCS single board computer can be operated stand-alone and it does not require a network connection in order to perform the basic control tasks. This feature is especially important in terms of safety requirements where a proper and secure operation of the detector has to be guaranteed even in cases where part of the higher levels of the control system are not working. During operation the Ethernet connection is required only for publishing measured data. It is also used in spy mode to access on-line data without affecting the main detectors data stream. This feature is very useful in particular during the debugging phase of the detectors and even during test measurements where performance is not essential.

Table 1: Usage of the Flash ROM

ARMboot	128 kByte
Linux kernel	630 kByte
root file system, including standard Linux tools, web server, telnet server, NFS	1.5 MByte
user applications	> 1.5 MByte

The usage of the Flash ROM is shown in Table 1. Assuming a size of the Flash ROM of 4 MByte, more than 1.5 MByte are available for user applications like DIM server or programs controlling the front end electronics. Obviously there are larger Flash ROM devices available. This small version was chosen for cost reasons.

III. ETHERNET AS FIELD BUS

A. Ethernet in Magnetic Field

One important task of the detector control system is the collection of data at the detector level and the distribution of these data to upper levels in the control hierarchy. Furthermore, data has to be sent to the front end electronics and the functionality for manual operator intervention is needed. All this requires a reliable field bus. One possible network technology which is discussed very actively in industry at the moment is Ethernet as field bus. One advantage of using Ethernet is its wide use and therefore the availability of cheap standard components. However, if used as field bus there are additional requirements which have to be fulfilled. The proper function of Ethernet even in a harsh environment with electromagnetic background noise has to be ensured. In case of ALICE (like in most other experiments in high energy or heavy ion physics) there is an additional complication due to the high magnetic field used for particle deflection. This complicates the use of standard network devices since they use a transformer for signal coupling. In case of the DCS single board computer this problem is solved by replacing the transformer with a small amplifier circuit which boosts the output signal of the physical layer chip. Since the physical layer chip uses the reflected signal for detecting and verifying the network cable a special feedback loop was added to the amplifier. The circuit is shown in Figure 4. First measurements were done with a setup consisting of a DCS single board computer and a standard switch with a 50 m UTP CAT5 cable between two devices and verified the proper function of the modification.
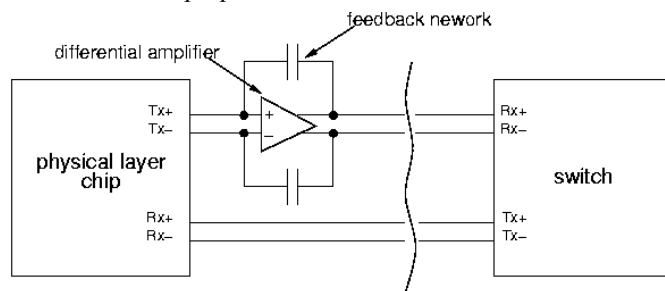

Figure 4: Modification of standard Ethernet to operate in magnetic fields. The transformer, which is typically used for electric decoupling, is replaced by a small circuit containing a differential amplifier with feedback network.

It should be noted here that other techniques were studied as well. For instance, the Ethernet signals could be converted optically. Various signal conversion standards and technologies were studied including the very low-cost TOSlink, used in the audio industry. However, for the TPC and TRD system where about 1000 of the discussed single board computers are required there was still a significant price difference as compared to the presented solution.

B. Easynet

Various commercial network interfaces exist. However, it soon became obvious that the required functionality can be implemented in a minor fraction of the already available FPGA resources, allowing to eliminate the appropriate external chip. In addition, plans exist to complement the existing Ethernet protocol with quality of service functionality, allowing the reservation of bandwidth and implementing high priority, reliable messages. Such functionality can be integrated and operated with existing commercial switches, provided that all participating MACs adhere to such functionality. The DCS single board computers will always operate in a closed subnet in which by definition all interfaces are alike. Therefore, such voluntary add-on functionality is very feasible. However, in that case the interface is required to be programmable and therefore was implemented as soft core in the FPGA.
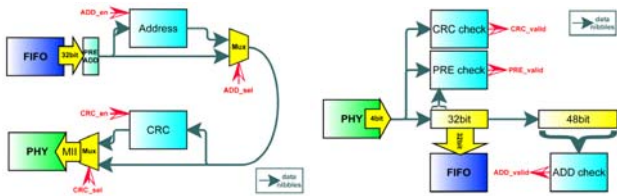

Figure 5: Data flow of the sender (left) and receiver (right) of the Easynet MAC.

Easynet is the realization of a simplified medium access controller (MAC) as a synthesizable module in VHDL [5]. The aim was an easy to use Ethernet interface for so-called *System on Chip* (SoC) applications. Since resources on programmable chips are always a limiting factor a simplified version of the Ethernet protocol was implemented in order to reduce the amount of required logic cells. Easynet works in full duplex mode only with transfer rates of 10 or 100 Mbit/s. It does not implement collision detection and therefore Easynet network devices have to be connected using a network switch. Nevertheless, considering the mentioned limitations Easynet devices behave as normal Ethernet devices. Figure 5 show the block diagrams of the transmitter and receiver parts of Easynet. Data packets are transferred between the physical layer chip and the Easynet MAC via the standardized medium independent interface (MII). The interface to the CPU is implemented as a FIFO. A simple state machine (comprising only 5 states for the receiver) controls the data flow. If synthesized for a FPGA the complete MAC requires approx. 1000 logic elements only compared to approx. 2500 LE for the fully feature MAC of the OpenCore project [6] and 4000 LE for Alteras' IP core.

IV. PROTOTYPE

Figure 6 shows a photo of the first prototype to the DCS single board computer. Besides the FPGA with ARM core the board is equipped with 4 MByte FLASH ROM which is used to store the FPGA configuration and the software, including Linux kernel and user applications. The systems main memory consists of an SDRAM chip with 32 MByte capacity. The Ethernet connection is realized with an Intel physical layer chip and the discussed differential amplifier. For flexibility the standard transformer may also be used. In addition to this core system the board contains an 8 channel, 16-bit ADC which is used for monitoring the operation parameters of the detectors. The global clock and trigger information is received with an optical fibre and processed with the TTCrx chip [7] developed at CERN. A standard SO-DIMM connector was chosen as interface to the detector. This allows for a simple but reliable low-cost mechanical and electrical connection.
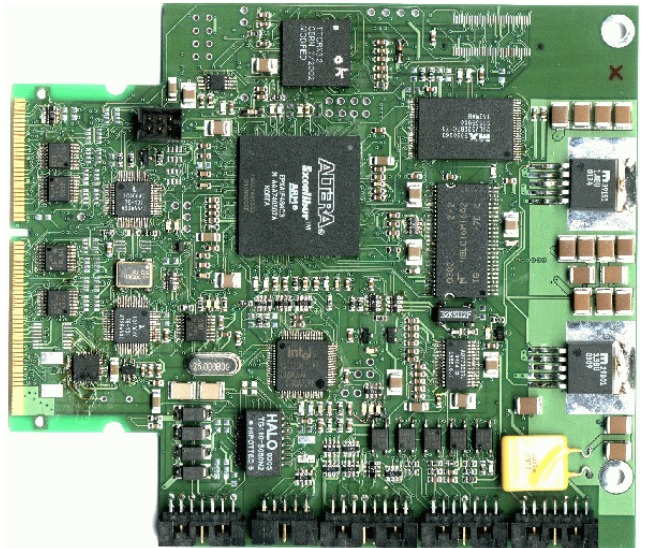

Figure 6: Prototype of the DCS single board computer.

Table 2: Key parameters of the DCS single board computer.

CPU	ARM922T, 32-bit RISC
FPGA	100,000 gates (1,000,000 optional)
	4160 Logic elements (LE) (38400 optional)
SDRAM	32 MByte
Flash memory	4 MByte (8 MByte optional)
ADC	8 channel, 16-bit
Power consumption	< 4 W

Table 2 above summarizes the overall features of the board. The total power consumption depends on the FPGA configuration and processor operation. Typical measurements, including all features of the DCS single board computer remained below 4W. A good fraction of the power is converted in the voltage regulators which generate the various supply voltages required from the single power supply voltage of 4 V.

V. RADIATION TESTS

Since the DCS single board computer has to operate in an environment with high radiation exposure special care has been taken during the design process to ensure radiation hardness and fault tolerance. For instance the entire clock circuitry is based upon radiation hard devices and is entirely independent of the rest of the device. This ensures that the clocks of the detectors and the device itself remain operational under all circumstances.

During first preliminary tests all major components of the board have been irradiated at the Oslo Cyclotron Laboratory with a 28.5 MeV proton beam. The beam currents varied between 10 and 100 pA. Using first simulations for the expected radiation within the ALICE detectors, the expected radiation during 10 years of operation can be applied in a few seconds.

First tests have been done with the Flash ROM. The ROM was programmed with test data and continuously read out. The retrieved data were compared to the original data and the number of bit-flips as a function of time recorded. First results show practically no errors up to beam currents of 100 pA. After increasing the beam current to 1 nA bit errors occurred after an irradiation time of 150 s which is many orders of magnitude beyond the expected radiation exposure in ALICE. Note that after observing such bit errors the FPGA devices could not be reprogrammed.

VI. REFERENCES

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