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Review Article

Industrial Silicon Wafer Solar Cells

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In 2006, around 86% of all wafer-based silicon solar cells were produced using screen printing to form the silver front and aluminium rear contacts and chemical vapour deposition to grow silicon nitride as the antireflection coating onto the front surface. This paper reviews this dominant solar cell technology looking into state-of-the-art equipment and corresponding processes for each process step. The main efficiency losses of this type of solar cell are analyzed to demonstrate the future efficiency potential of this technology. In research and development, more various advanced solar cell concepts have demonstrated higher efficiencies. The question which arises is "why are new solar cell concepts not transferred into industrial production more frequently?". We look into the requirements a new solar cell technology has to fulfill to have an advantage over the current approach. Finally, we give an overview of high-efficiency concepts which have already been transferred into industrial production.

1. INTRODUCTION

The photovoltaic industry has produced 2.54 GW of solar cells in 2006 [1]. 89.9% of these cells were made from mono- and multicrystalline silicon wafers, 7.4% from thin films (a-Si, CdTe, CIS), and 2.6% from silicon ribbons (EFG, string ribbons). In 1975, screen printing was first applied to solar cells for the formation of the front and rear contacts replacing expensive vacuum metallization [2]. In 2006, around 86% of all produced wafer-based silicon solar cells are still featuring screen-printed front and back contacts. Since 1975, process and equipment for the screen-printed solar cell has been further optimized and new technologies have been introduced to improve this technology. (i) Silicon nitride as an antireflection coating with excellent surface and bulk passivation properties [3]. (ii) Texture of the front surface to reduce reflection of mono- and multicrystalline silicon [4, 5]. (iii) Laser edge isolation and single-side etching for the electrical separation of the front and rear contacts [6, 7]. Today the standard screen-printed solar cell reaches average efficiencies of around 15% for multicrystalline and of around 16.5% for Czochralski silicon in the industry. Various research groups all over the world have been working on more advanced solar cell concepts and they successfully reached efficiencies well above 20% [8–10]. However, only a few of these more advanced technologies were introduced into industrial production [11–15] having a market share of 14% of all wafer-based silicon solar cells in 2006.

In this article, we will look into processes and equipment currently used to produce standard screen-printed solar cells. We will then analyze the main optical and electrical losses occurring in this type of solar cell before we give an overview on more advanced solar cells with a higher efficiency potential produced by a few companies. Furthermore, we will look into the requirements a new solar cell technology has to fulfill to be used by the photovoltaic industry.

2. SCREEN-PRINTED SILICON SOLAR CELLS

Most screen-printed solar cells fabricated in the industry today are using the process sequence summarized in Table 1. This sequence consists of a relatively small number of process steps. Process equipment for this type of solar cell is commercially available, with a variety of different equipment and consumable manufacturers. A schematic drawing of this type of solar cell is shown in Figure 1. Today, the standard screen-printed solar cell reaches average efficiencies of around 15% for multicrystalline and around 16.5% for Czochralski silicon in industrial production. In the following sections, the process and most commonly used equipment for each process step is summarized.

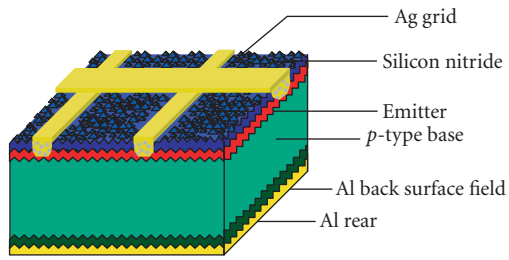


Figure 1: Schematic drawing of a solar cell with a silicon nitride antireflection coating and a screen-printed silver front and aluminum rear contacts.

Table 1: Process sequence for screen-printed solar cells.

(1)	Saw damage removal, texture, and cleaning of *p*-type silicon wafer
(2)	Phosphorus diffusion
(3)	Plasma edge isolation (alternatively, this process is often replaced by a single-side etching step integrated into the wet bench for phosphorus glass removal or by laser edge isolation placed after the firing step)
(4)	Phosphorus glass removal (and single-side etching for edge isolation)
(5)	Silicon nitride deposition
(6)	Ag screen printing of the front contact and drying
(7)	Al/Ag screen printing of the rear busbars and drying
(8)	Al screen printing of the rear and drying
(9)	Cofiring of the front and rear contacts
(10)	IV measurement and sorting

2.1. Saw damage removal, texture, and cleaning

Wire sawing is used to cut silicon ingots into wafers. This process induces small cracks penetrating around 10 μm deep into the wafer surface as shown in the left cross-section image of Figure 2. Saw damage has to be removed from the wafer surface, because it reduces the mechanical strength of the wafer and increases recombination in the surface region. Alkaline [4, 16, 17] or acidic [5, 18, 19] solutions as well as plasma etching can be used for saw damage removal. In addition, this process step is normally used to form a surface texture that reduces the total reflection of the wafer. After etching, the wafer is cleaned to remove metal and organic contaminants that would cause an increase of surface and bulk recombination during the following high-temperature process steps.

A solution of sodium hydroxide NaOH or potassium hydroxide KOH and water is normally used for alkaline saw damage removal on multi- or monocrystalline silicon wafers. The etching reaction can be summarized as $Si + 2H_2O + HO^- \rightarrow HSiO_3^- + H_2$ and takes place in three reaction steps: (i) oxidation of silicon; (ii) formation of a solvable salt; and (iii) dissolving of the salt in water.

Alkaline etching has different etch rates for different crystallographic orientations. This anisotropy results in small pyramids with a square base randomly distributed over the wafer surface for monocrystalline silicon wafers with a (100) surface orientation. To improve the lateral uniformity and the anisotropy of the etching process, isopropyl alcohol (IPA) is added to the etching solution. Applying this texture the total reflection of a polish-etched planar, silicon wafer can be reduced from 35 to 12% [4].

After texturing, the wafers are rinsed in deionized (DI) water, cleaned in hydrochloric acid (HCl), rinsed in DI water, cleaned in hydrofluoric acid (HF), rinsed in DI water, and finally dried in hot air. HCl removes metal impurities from the wafer surface. HF etches the native silicon dioxide off, removes metals with this surface, and forms a hydrophobic surface.

Alkaline saw damage removal, texture, and cleaning are performed in batch processes. Wafers are held in cassettes that allow chemicals to wet the entire surface. These cassettes are moved automatically from one to the other tank filled with chemicals and water for etching, cleaning, rinsing, and drying. For process control, the loaded cassettes are weighed before and after etching to determine the etching depth from the difference in weight.

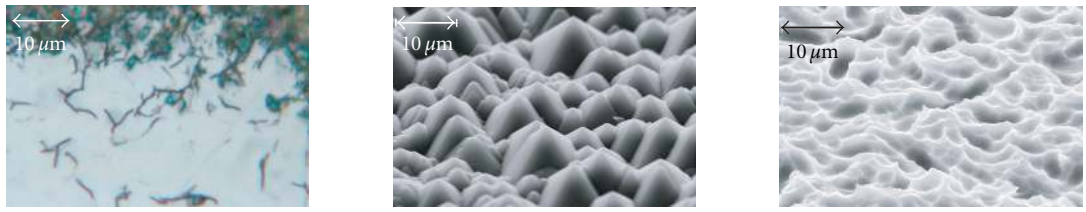
Acidic texturing is an isotropic process. It is not dependent on the crystallographic orientation and it is therefore suited for saw damage removal and texturing of multicrystalline silicon. A solution of HF, nitric acid (HNO_3), and water was introduced for saw damage removal and texture of multicrystalline silicon wafers [4]. The reaction takes place in two reaction steps: (i) oxidation given as $3Si + 4HNO_3 \rightarrow 3SiO_2 + 2H_2O + 4NO$ and (ii) etching of silicon oxide given as $3SiO_2 + 18HF \rightarrow 3H_2SiF_6 + 6H_2O$

Batch and inline equipment is commercially available for the acidic texture. For the inline process, the wafers are moved horizontally on rolls through tanks. For cleaning, DI water is sprayed onto the wafers. A typical process sequence is as follows: (i) saw damage removal and texture in H_2O, HNO_3, and HF, (ii) spray rinse, (iii) KOH to etch porous silicon off that was formed during acidic texture, (iii) spray rinse, (iv) HCl clean, (v) spray rinse, and (vi) air drying. The etching time of commercial equipment is around 2 minutes per wafer adding up to around 2000 wafer/h for $156 \times 156\,mm^2$ wafers.

The solar cell efficiency depends strongly on the etching depth of the acidic texture. If the etching depth is too shallow, crystal defects remain and the open-circuit voltage as well as the short-circuit current is reduced. If the etching depth is too deep, the surface roughness increases decreasing the open-circuit voltage and short-circuit current (increased surface recombination). The best solar cell efficiency has been found for an etching depth between 4 to 5 μm [18]. A solar cell efficiency improvement of 7% relative has been demonstrated if acidic-etched wafers were used instead of NaOH-etched wafers [19, 20]. Figure 2(c) shows a SEM microscopic surface image of an acidic-textured multicrystalline silicon wafer.

2.2. Diffusion

Most commonly used in the photovoltaic industry is a tube diffusion process. The wafers are vertically placed into a quartz boat. The boat moves into a quartz tube and is heated up to around 800 to 900°C. Nitrogen flows as a carrier gas



(a) (b) (c)

Figure 2: (a) Cross-section image of a wafer after wire sawing. (b) Top view of a wafer after alkaline texture in KOH, IPA, and water forming random pyramids. (c) SEM microscopic image of the surfaces of an acidic-textured multicrystalline silicon wafer [19].

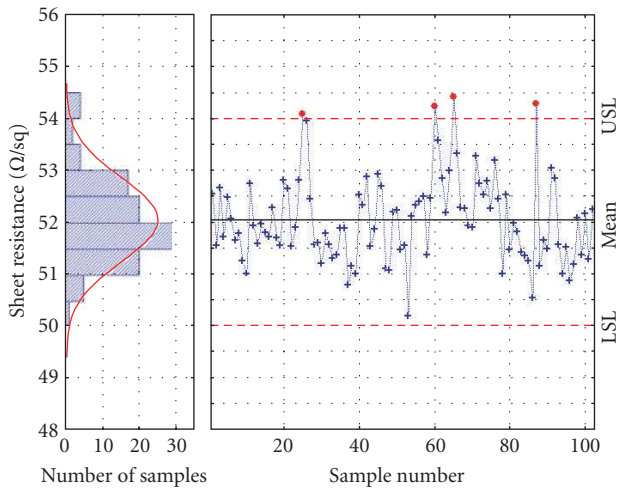


Figure 3: Control chart of the emitter sheet resistance measured with a contact-less inline method with the upper (USL) and lower specification limit (LSL) for the sheet resistance.

through a bubbler filled with liquid phosphorus oxychloride $POCl_3$. The formed gaseous $POCl_3$ is mixed with O_2 and conducted directly into the heated quartz tube. Phosphorus oxide P_2O_5 deposits onto the wafer surfaces. The released Cl_2 removes metal impurities. At the involved temperatures, phosphorus diffuses into the silicon forming a *pn* junction with the *p*-type base.

An alternative method is the deposition of diluted phosphoric acid H_3PO_4 onto the wafer surface. The wafer moves horizontally on a conveyer belt through mist consisting of H_3PO_4 and water. The drive-in of the phosphorus is performed on a conveyer belt firing furnace [21].

For the standard screen-printed solar cell, an emitter sheet resistance of 40 to 60 Ω/sq is normally in use. Figure 3 illustrates a control chart for the emitter sheet resistance measured with a contact-less inline method.

Phosphorus diffusion reduces the concentration of impurities by gettering. Impurity gettering is improved by increasing the diffusion time and reducing the peak temperature if the sheet resistance has to stay the same [22]. Additionally, it was shown that a double-sided diffusion gives better efficiencies than a single-sided diffusion [23].

2.3. Phosphorus glass removal and edge isolation

Phosphorus glass on the wafer surface is etched off using HF. It is very common to use a batch wet bench for this process. Most recently, inline equipment became commercially available to remove the phosphor glass. In addition, this equipment can perform single-side etching on the wafer to remove the emitter from one side [24]. The solar cell is transported on the surface of an etching bath in such a way that only the back side of the wafer is wetted. Using a solution of H_2O, HF, HNO_3, and H_2SO_4, the emitter is completely removed from the back side of the wafer. Consequently, the front and the rear sides of the solar cell are electrically isolated. The single-side etch is therefore an alternative process to plasma etching or laser edge isolation [7, 25, 26].

2.4. Silicon nitride deposition

A layer of silicon nitride SiN_x:H with up to 40 at% of hydrogen [3] is deposited onto the front side of the solar cell as an antireflection coating. After screen printing, the Ag contacts are fired through the SiN_x:H layer. To minimize optical losses, the SiN_x:H film has a thickness of around 75 nm and a refractive index of around 2.05. In addition, SiN_x:H serves as a good surface passivation to reduce recombination losses of the emitter [27–29]. Furthermore, hydrogen is released from the hydrogen-rich SiN_x:H film during a postdeposition anneal reducing bulk recombination in multicrystalline silicon [29, 30]. For the first screen-printed silicon solar cells, titanium dioxide TiO_2 or thermally grown silicon dioxide SiO_2 was used as an antireflection coating. However, TiO_2 has no surface or bulk passivation properties; and the refractive index of SiO_2 is too low for optimal optical performance [3]. The surface passivation properties of SiO_2 are excellent, but it does not passivate bulk defects in multicrystalline silicon. Furthermore, oxidation requires high temperatures creating additional defects within multicrystalline silicon and reducing equipment throughput.

Today, plasma-enhanced chemical vapor deposition (PECVD) is most widely used in the photovoltaic industry to deposit SiN_x:H as an anti reflection coating. The PECVD method was invented in the field of microelectronics by Sterling and Swann in 1965 [31]. In 1981, the PECVD

method was first applied to solar cells by Hezel and Schörner [32]. Kyocera in Japan was the first company that used the PECVD method commercially for screen-printed multicrystalline silicon solar cells achieving good optical properties as well as good surface and bulk passivation [33]. A good overview of various SiN_x:H deposition techniques, its surface, and bulk passivation properties and its application to solar cells is given by Aberle [34] and Duerickx and Szlufcik [3]. Generally, there are four basic methods to form SiN_x:H films: (i) plasma-enhanced chemical vapour deposition (PECVD); (ii) atmospheric pressure chemical vapor deposition (APCVD); (iii) low-pressure chemical vapor deposition (LPCVD); and (iv) sputtering.

In the PECVD process, the deposited SiN_x:H film is formed in a reaction of silane SiH_4 and ammonia NH_3 at a temperature between 200 and 450°C and a pressure between 0.1 and 1 mbar. In *direct* PECVD, the process gasses are excited by an alternating electromagnetic field where the wafers form the electrodes. In batch systems, the wafers are loaded into graphite boats acting as electrodes. The wafers are processed in a quartz tube. An alternative approach is the *remote* PECVD process. For this method, the plasma excitation is spatially separated from the wafer. A linear plasma source is used, in which microwaves from an external source are coupled into the process chamber. The wafers are loaded onto CFC carriers and are moved horizontally through the plasma chamber. Direct and remote PECVD systems have the highest market share in the photovoltaic industry, because of their high throughput and low process temperatures.

In the LPCVD process, dichlorosilane SiH_2Cl_2 and ammonia NH_3 are used to form the SiN_x:H film on the wafer surface at a pressure between 0.01 and 1 mbar and temperatures around 750°C. SiN_x:H films deposited by means of the LPCVD method have a much lower hydrogen content than films deposited with the PECVD method. Consequently, the PECVD process is better suited for the bulk passivation of multicrystalline silicon. LPCVD batch systems are commercially available with a lower throughput than PECVD systems, because of the required cooling time for the process temperature of 750°C.

In the APCVD process, the chemical reaction takes place between silane SiH_4 and ammonia NH_3 at temperatures between 700 and 1000°C and atmospheric pressure (1000 mbar) to deposit SiN_x:H films. The APCVD method is mostly used in microelectronics.

Recently, it has been demonstrated that sputtered SiN_x:H films achieve similar surface and bulk passivation properties as SiN_x:H films deposited by PECVD [35, 36]. For this process, wafers are moved horizontally on a CFC carrier through the inline system. Two boron-doped silicon targets are alternately sputtered in argon and nitrogen using a mid-frequency power supply to deposit SiN_x onto the silicon wafer. By adding reactive gases like H_2 or NH_3, the refractive index and the hydrogen content of the SiN_x:H layer can vary independently. For the sputter deposition of SiN_x:H, a temperature between 350 and 400°C and a base pressure of 0.001 to 0.03 mbar are used.

2.5. Screen printing of the front contact

Screen printing has its origins in stencil printing, a method which has already been used 1000 years ago. Stencil printing did not allow printing closed inside patterns such as the character "O." The idea of screen printing developed when loose parts of the stencil where connected with fine wires. Later, the fine wires were replaced by a screen with area-blocked and area-open spaces where the ink can go through. Screen printing is extensively used for textile printing. During the 2nd World War, electronic circuit boards were manufactured using this technology. In 1975, screen printing was first applied to solar cells for the formation of front and rear contact printing Ag and Al pastes, respectively [2]. Today, screen-printing equipment for the formation of the front and rear contacts of solar cells is commercially available, with various manufactures for equipment, screens, and pastes. Screen-printing equipment is robust, simple, and can easily be automated. Most commercial screen printing lines have a net throughput of around 1000 and 2000 wafers/h for single and double lines, respectively. Solar cells up to $210 \times 210\,mm^2$ in size can be processed on these lines.

The silicon wafer is moved on a conveyor belt or walking beam onto a printing table. The screen mounted into an aluminium frame has areas that are blocked off with a stencil (positive of the front grid to be printed) and areas that are open where the paste will go through later on. The screen is positioned and placed on top of the front side of the wafer with a defined distance between wafer and screen (snap-off distance). In the next step, a squeegee is moved without pressure over the screen to fill the screen openings uniformly with Ag paste (flooding of the screen). The squeegee is then moved with a defined pressure over the screen pressing the screen locally against the wafer surface and pushing the Ag paste from the filled areas of the screen onto the wafer surface. Due to the screen tension, the screen snaps off from the wafer in all areas where the squeegee is not pressing the screen against the wafer. After printing, the wafer is transported on a conveyor belt or walking beam through a drying furnace before being placed onto the next printing table for printing the rear side. At the end of the printing process, the front and the rear contacts are fired simultaneously in a firing furnace. A discussion of the impact of the different printing parameters on the quality of the print is given by Holmes and Loabsy [37].

The screen-printed front contact has to have the following features: (i) low contact resistance; (ii) no junction shunting; (iii) low specific resistance; (iv) high aspect ratio; (v) good adhesion to silicon; (vi) firing through SiN; and (vii) good solderability for series interconnection with tabbing ribbons within the module.

The Ag paste for the formation of front contacts consists of (i) Ag powder (70 to 80 wt%), (ii) lead borosilicate glass PbO-B_2O_3-SiO_2 (1 to 10 wt%), and organic components (15 to 30 wt%). The Ag powder sinters during firing and causes good lateral conductivity of the fingers. The PbO-B_2O_3-SiO_2 frits are essential for the contact formation during

firing. PbO-B_2O_3-SiO_2 etches through the SiN antireflection coating, promotes the adhesion of the Ag contact to the silicon, reduces the melting point of Ag, and prevents Ag to diffuse into the *pn* junction causing junction shunting and space charge region recombination. However, the PbO-B_2O_3-SiO_2 layer formed between the conducting finger and the emitter is also the reason for the poor contact resistance of the screen-printed Ag contact [38]. The organic components determine the rheology of the paste. The viscosity of the paste reduces with the impact of squeegee movement to be extracted easily from the screen, it has to stay at a low-viscosity level to form a continuous finger (no string of pearls appearance), but then the viscosity has to increase again to keep a high aspect ratio and avoid that the finger flows apart [39].

The current understanding of contact formation and current transport of screen-printed contacts are given by Ballif et al. [40, 41] and Schubert et al. [38, 42, 43]. Below 600°C, the organic components burn out. Above 600°C, the contact formation takes place.

(1) Lead borosilicate glass melts, wets, and etches the SiN surface while the Ag particles sinter to a conductive film.

(2) A redox reaction between PbO and Si takes place forming liquid Pb. Ag and Si dissolve in liquid Pb etching inverted pyramids into the wafer surface.

(3) During cooling, Ag and Pb separate according to the phase diagram. The Ag recrystallizes epitaxially in the inverted pyramids forming Ag crystallites at the wafer-glass interface. The Ag crystallites form isolated ohmic contacts to the emitter. Note that the sintered Ag thick film is separated from the emitter by a glass layer.

(4) The current transport between these Ag crystallites into the sintered Ag thick film is assumed to take place at interconnections between crystallites and the sintered film, tunneling through ultra thin glass regions or multistep tunneling via metal precipitates that are formed in the glass layer during cooling.

2.6. Screen printing of the aluminium rear contact

The same screen printing equipment used for printing the front side is applied as well for printing the rear side. However, Al paste is used for the formation of a good ohmic rear contact and an Al back-surface field (BSF) to *p*-type silicon by Al doping of the rear surface region during firing. The doping profile and thickness of the BSF, the back surface reflectivity, the BSF homogeneity, and the wafer bow depend critically on the amount of Al paste printed onto the rear side of the wafer (between 6 and 10 mg/cm^2 of dried Al paste), the peak firing temperature, the type of paste and sufficient oxygen supply during firing [44]. A model for the formation of the screen-printed rear contact is given by Huster [44]. It follows a description of his model according to the numbers in Figure 4.

(1) Al paste consists of Al powder, a glass frit to enhance sintering, and organic binders and solvents. After drying, a porous paste matrix covers the wafer surface. With the further temperature increase the organic binders burn out.

(2) Melting of Al starts at 660°C which can be observed in a small plateau (latent heat). The aluminium oxide Al_2O_3 surfaces of the Al particles stay in shape during the entire formation process. However, liquid Al penetrates through the Al_2O_3 surface locally and gets in contact with the wafer surface and other Al particles. The wafer surface is not fully covered with Al at this stage.

(3) Soon after melting, all Al paste particles reach thermal equilibrium. According to the phase diagram shown in Figure 4, more and more Si is dissolved in liquid Al with increasing temperature. The volume of the Al particles is limited by the Al_2O_3 skin and stays therefore constant. If Si gets dissolved in the Al particles, the same volume of Al is transported out of the particles to the wafer surface.

(4) At peak temperature, the entire wafer surface is covered with liquid Al-Si with exactly the same volume as that of the dissolved Si.

(5) During cooling down, the process (3) occurs in reverse direction, that is, Si is rejected from the melt to recrystallize epitaxially on the wafer surface building up the Al-doped layer (Al BSF).

(6) After reaching the eutectic temperature of 577°C, the remaining liquid phase solidifies instantly. The Al particles have the eutectic composition with 12% Si dissolved, a certain amount of Al is found on the wafer surface between the BSF and the film of Al particles.

2.7. Screen printing of the rear busbars

It is not possible to solder onto the screen-printed Al contact. Therefore, an Ag or Al/Ag paste is used to print busbars that can easily be soldered to tabbing ribbons for series interconnection to modules. It is important that the rear busbars or pads are kept as small as possible to reduce additional efficiency losses (no BSF underneath the Ag busbars), but that they are kept large enough to allow misalignments in the soldering process.

2.8. Firing

After screen printing, the front and the rear sides as described above with Ag and Al are fired simultaneously in a firing furnace (cofiring). The firing process is an inline process with the solar cells placed horizontally onto a metal conveyor belt. The furnace has several zones that can be heated up to 1000°C separately with IR heaters. The wafers can be heated from the front and the back, some furnaces have additional side heaters to adjust the lateral temperature uniformity. Firing furnaces are operated with a set air flow and exhaust. A simulated temperature profile for firing wafers is shown in Figure 4 featuring a

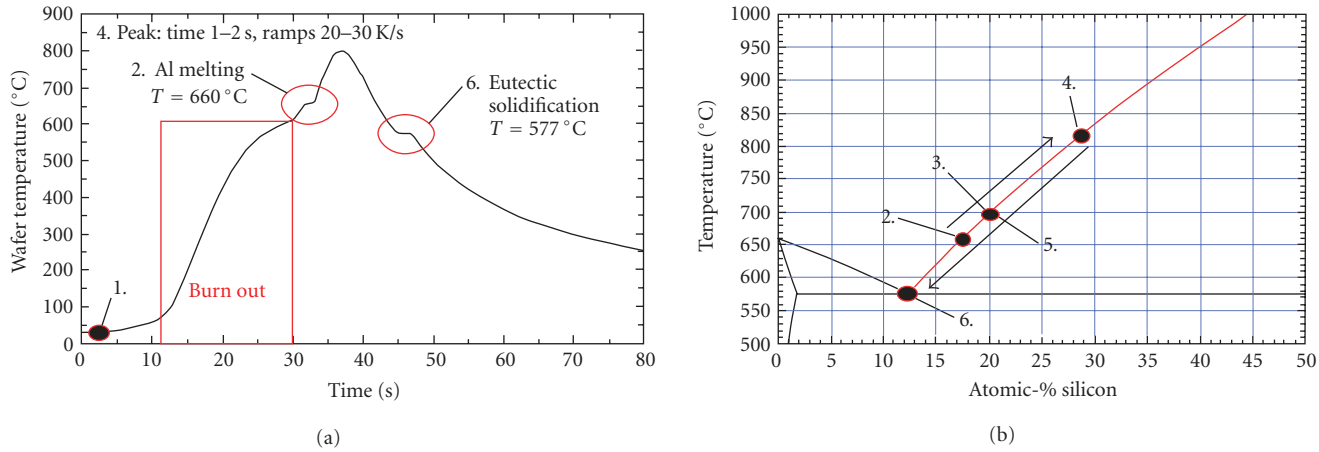


Figure 4: (a) Calculated temperature profile for firing Al paste through a silicon nitride layer and Al paste to form the rear contact of a silicon solar cell in a belt furnace [44]. (b) Calculated binary phase diagram of Al Si [44]. The distinctive points during the formation process are labeled in both graphs.

burn-out zone to burn organic binders and a sintering zone with a set peak temperature. In this zone, the front contact (firing through SiN, contact sintering, formation of the ohmic contact) and rear contact (BSF formation, contact sintering, formation of the ohmic contact, Al gettering) are formed and the hydrogen of the SiN_x:H layer is released into the bulk of the wafer to passivate electrical defects. Profiling systems to record the temperature of a wafer traveling through the firing furnace are commercially available [45].

2.9. IV Measurement and sorting

At the end of the solar cell manufacturing process, the IV characteristics and the optical parameters of each individual solar cell are measured. The reason for this is (i) to determine the optical quality, (ii) to determine its current at the maximum power point and sort the cells into current classes to minimize mismatch losses in the module consisting of series-connected solar cells [46], (iii) to determine its reverse break through characteristics to avoid hot-spot heating within the module [47], and (iv) to determine solar cell parameters such as *Eta*, V_{oc}, J_{sc}, and *FF* as a final process control.

Most IV testers consist of a halogen flash lamp that can stay constant for more than 50 milliseconds (1000 W/m^2, reproducibility ±1.5%, spectra class A, and uniformity of ±2% after IEC60904-9). The IV characteristics are measured by a current-voltage curve tracer using a four quadrant power supply. The temperature of the solar cell is measured. A monitor cell is used to track changes in light intensity of the flash. The IV curves are measured using a four-point probe and they are corrected for changes in temperature and light intensity to 1000 W/m^2 and 25°C, respectively. It is important that IV testers are frequently calibrated using certified reference solar cells so that reproducibility can be controlled frequently [48].

3. ELECTRICAL AND OPTICAL LOSSES OF SCREEN-PRINTED SOLAR CELLS

Screen-printed fingers of industrially produced solar cells have a typical pitch of around 2 mm and are between 120 and 160 μm wide. This, together with the two 2.0 mm wide busbars, causes a shading loss of around 8%. Research and development focus therefore on improving or replacing the current screen printing technology to achieve finer grid lines [49]. The internal back reflectance for a screen-printed Al contact is between 75% and 80% [44].

Currently, an emitter diffusion with a sheet resistance of around 40 to 60 Ω/sq and a surface doping concentration of above 2×10^{20} cm^{-3} is used to fabricate screen-printed silicon solar cells. The high surface doping and low sheet resistance is necessary to achieve an acceptable contact resistance of around 1.0×10^{-3} Ωcm^2 as well as low junction shunting and recombination in the space charge region. However, this type of emitter has low open-circuit voltages (high surface recombination for emitters with high surface doping and Auger recombination) as well as poor short-circuit currents caused by a poor blue response (high-emitter recombination and free-carrier absorption). Good screen-printed contacts with a contact resistance of around 1.0×10^{-4} Ωcm^2 to "high efficiency emitters" with a sheet resistance above 100 Ω/sq and a surface doping of around 1×10^{19} cm^{-3} are therefore the main task in developing high efficient industrial solar cells [38, 50, 51].

The specific line resistance of screen-printed fingers is around 3.0×10^{-6} Ωcm, its average width and height is 130 and 12 μm, respectively. The resulting line conductivity together with the contact resistance mentioned above results in average fill factors between 76% and 78%. For comparison, laboratory high efficiency solar cells using photolithography to define evaporated Ti/Pd/Ag contacts on selective emitters reach fill factors between 81% and 82% having a finger width of 20 μm, a finger height of 8 μm, a

specific finger resistance of $1.7 \times 10^{-6}\,\Omega$cm, and a contact resistance of $1.0 \times 10^{-5}\,\Omega\text{cm}^2$.

Fischer [52] determined for a 15% efficient multicrystalline silicon solar cell that only 31.8 mA/cm^2 (its short circuit current density) of the 35 mA/cm^2 generated in this solar cell are collected. These recombination losses occur with 41% in the base, 34% in the emitter, and 25% at the rear surface. In addition to these losses in short-circuit current, injected minority carriers are lost at the maximum power point (saturation current losses). Fischer [52] calculated for the 15% efficient multicrystalline silicon solar cell at the maximum power point additional losses of 2.15 mA/cm^2. 34% of these losses occur in the space charge region, 26% in the emitter, 25% in the base, 12% at the rear, and 4% via shunt resistances.

4. REQUIREMENTS FOR A NEW SOLAR CELL TECHNOLOGY

Equipment, labor, land, and material costs, sales prices as well as technological aspects influence the return of investment of a company. Technology has an impact on (i) the solar cell, module, and system efficiency; (ii) the yield of the process; (iii) fixed costs; (iv) variable costs; and (v) the system lifetime.

4.1. Efficiency

Improvements of the cell, module, or system efficiency reduce the cost in all process steps (wafer, cell, module, and balance of system), because most of the costs are area-related. Consequently, if the efficiency improves by a factor of α, the production costs per watt decrease by a factor of $\beta = 1/\alpha$ if everything else remains unchanged. Table 2 shows the overall cost improvements β associated with an efficiency improvement $\alpha = 1.1$ in wafer, cell, or module manufacturing assuming no additional costs associated with this innovation. Rogol and Conkling [53] rate the breakdown of costs for wafer, cell processing, module manufacturing, and balance of system as $w = 26.0\%$, $c = 16.6\%$, $m = 18.7\%$, and $s = 38.8\%$, respectively. However, sometimes it is more interesting to know the maximum price for an improvement that is acceptable. Using (1) allows us to calculate the cost limit γ; a new technology should not exceed if a power improvement of $\alpha = 1.1$ is reached. The corresponding cost limit γ for wafer, cell, and module manufacturing is given in Table 2. If higher costs occur, the technology currently used is more cost-effective. Note that w, c, m, and s correspond to the breakdown of costs before the technology was changed,

$$\gamma_W \le \frac{\alpha - c - m - s}{w},$$
$$\gamma_C \le \frac{\alpha - w - m - s}{c}, \tag{1}$$
$$\gamma_M \le \frac{\alpha - w - c - s}{m}.$$

Very often, new developments to improve the solar efficiency are very expensive. Ready-made equipment does not exist. A company has to develop its own process and equipment resulting in process sequences with more process steps, expensive equipment, and a low yield. Moreover, the screen printing technology has improved dramatically in yield and efficiency over the last years. These uncertainties are a burden for the introduction of new technologies.

4.2. Yield

The yield of the overall manufacturing process from the wafer to the module is reduced by (i) wafer breakage, (ii) electrical losses such as solar cells with shunts or efficiencies below a threshold value, and (iii) solar cells that do not meet the optical requirements (color of antireflection coating, paste stains, etc.). The value of a wafer increases with each manufacturing step. Consequently, a wafer that gets lost during wafering has a smaller impact on the overall costs than a wafer that gets lost during module manufacturing. Equation (2) can be used to calculate the cost reduction β of the overall system costs using the yield improvement in wafering α_W, cell processing α_C, and module manufacturing α_M as well as the cost breakdown of wafer, cell, module, and balance of system:

$$\beta = \frac{w + \alpha_W c + \alpha_W \alpha_C m + \alpha_W \alpha_C \alpha_M s}{\alpha_W \alpha_C \alpha_M}. \tag{2}$$

In a similar way as shown for efficiency improvements, it is possible to calculate the cost limit γ an innovation should not exceed, if a yield improvement is reached in wafer production α_W, cell processing α_C, and module manufacturing α_M as shown in (3):

$$\gamma_W \le \frac{1 - c - m - s}{w}\alpha_W,$$
$$\gamma_C \le \frac{(1 - m - s)\alpha_C - w}{c}, \tag{3}$$
$$\gamma_M \le \frac{(1 - s)\alpha_M - w - c}{m}.$$

If higher costs occur for an innovation in wafering γ_W, cell processing γ_C, and module manufacturing γ_M, the technology currently used is more cost-effective. Using (2) and (3), a yield improvement of $\alpha = 1.1$ as well as the cost breakdown of Rogol and Conkling [53] for wafers w, cells c, modules m, and balance of system s, the cost reduction β, and the corresponding investment limit γ is shown in Table 2. It is clearly visible that the cost reduction increases with the value of the wafer within the value chain. The yield will be reduced with the introduction of thinner wafers for example. Estimating the yield reduction in wafering α_W, cell processing α_C, and module manufacturing α_M allows you to estimate the required cost improvement in wafering γ_W, cell processing γ_C, and module manufacturing γ_M.

4.3. Fixed costs

The costs for each process step can always be divided into fixed costs and variable costs that depend on the

Table 2: Calculation of the cost improvement β associated with a power or yield improvement α in wafer, cell, or module manufacturing assuming no additional costs associated with this improvement as well as the cost breakdown of Rogol and Conkling for wafer, cell, module, and balance of system [53]. The technology cost limit γ gives the maximal cost increase that should be accepted for an innovation in wafer, cell, and module manufacturing. If higher costs occur, the technology currently in use is more cost-effective.

Improvement	Origin	Improvement α	Cost improvement β	Cost limit γ
Power	Wafer	1.1	0.909	1.385
Power	Cell	1.1	0.909	1.602
Power	Module	1.1	0.909	1.535
Yield	Wafer	1.1	0.976	1.100
Yield	Cell	1.1	0.961	1.256
Yield	Module	1.1	0.944	1.328

consumption of goods (wafers, consumables, gasses, etc.). Fixed costs consist of equipment costs (cost of specific equipment and number of process steps), footprint per installed capacity for the technology, clean room requirements, and labor requirements (number of process steps and level of automation). A new technology always has to pay for the market introduction, some equipment for advanced processing is more expensive than the standard technology and new technologies require many more process steps than currently used to produce standard solar cells.

4.4. Variable costs

Variable costs are all costs that depend on the consumption of raw materials and operating supplies. The consumption of these materials is related to the area of produced goods. If a new technology is able to process a thinner wafer than the current screen printing technology, this will reduce the cost of the raw materials. Furthermore, it is important for a new technology that the required consumables are unlimited. The price of Ag, for instance, has increased dramatically over the last years following a growing demand. Consequently, a new technology becomes more interesting if the consumption of Ag is replaced by cheaper materials.

4.5. Lifetime of the system

A technological change should not shorten the lifetime of the final system. Extensive module reliability testing will have to be performed for new technologies. Experience with screen-printed solar cells has now been gathered over the last 30 years. Therefore, it is very safe for the photovoltaic industry to stay with this technology.

4.6. Match to the current technology

It is a drawback for a new technology, if its implementation requires a change of all following manufacturing steps. For instance, the solar cell manufacturer introduces a back contact solar cell. Consequently, the module manufacturer has to change his entire fabrication method. This requires a larger investment and reduces the flexibility of the solar cell producer to sell his product to various costumers.

5. ADVANCED SOLAR CELL PROCESSES USED IN THE PHOTOVOLTAIC INDUSTRY

Various promising cell concepts from research and development are under investigation for commercialization. However, only a few more advanced solar cell technologies have already been introduced to industrial production. In the following, a short overview about the commercialized technologies is given first, followed by a more detailed description of the technologies.

Based on passivated emitter solar cells, the more industrial oriented technology of the laser-grooved buried contact (BC) solar cell was developed at the University of New South Wales, Australia, and licensed to a couple of companies. At BP Solar, a prominent representative of the licensees, a production was built up based on this technology and has produced up to 50 MW_p/a [53].

The application of a back surface field (BSF) was known for a long time; and conventionally the screen-printed and alloyed Al-BSF is state-of-the-art. The application of boron to form the BSF has a higher efficiency potential and allows the use of thinner wafers with less bow. This technology was applied by Siemens Solar and has produced up to 70 MW_p/a.

Another technological approach was the development of the heterojunction with intrinsic thin layer (HIT) solar cell by Sanyo, Japan. The peculiarity of the HIT solar cells is derived from the excellent passivation ability of the HIT structure on monocrystalline silicon. HIT cells reached already efficiencies above 20% and are fabricated by Sanyo in high volume production of about 170 MW_p/a [53].

In conventional solar cells, the metal coverage on the cell front side is a compromise between shadowing and series resistance losses. A complete contact free cell front side would help effectively for an efficiency improvement and therefore back contact solar cells were developed, where all contacts are located at the solar cell rear side. Hereby, around 9% front-side metallization coverage is avoided and thus the efficiency potential is increased by about 9% relative. Moreover, the back contact solar cells allow the decoupling of the front side for optical performance, low surface recombination, and low series resistance.

First designs of interdigitated back contact (IBC) solar cells were investigated by Lammert and Schwartz [14]. The development and commercialization on monocrystalline silicon were carried out by Swanson et al. and the SunPower

Corporation. Meanwhile back contact solar cells are in production by SunPower in the range of 60 MW_p/a [53].

With regard to the trade-off between resistive and optical shadowing losses in the back contact solar cells the transport of the high currents is carried out in interconnections on the rear side. The co-planar arrangement of *p* and *n* contacts on the rear side allows also a simplified cell interconnection. Moreover, IBC solar cells can be closer spaced allowing a higher packing density within the module. The most common separation of the *p* and *n* regions on the rear side is an interdigitated structure where the *p* and *n* regions alternate.

Other concepts of back contact solar cell designs like the emitter wrap through (EWT) and the metallization wrap through (MWT) solar cells have a fraction of the collecting emitter on the cell rear side and an additional second carrier collecting junction at the cell front side leading to higher current collection. The EWT solar cell structure is especially beneficial for lower quality crystalline silicon material. EWT solar cells are produced by Advent Solar Inc. (NM, USA). MWT solar cells are also capable for the application on lower quality silicon because of their emitter and metallization gridlines on the cell front side and the emitter and base contact on the rear side, however, only a moderate reduction of the front side shadowing is reached. MWT solar cells have not been transferred into large scale production yet.

5.1. Buried contact solar cells

The BC solar cell concept [11] was invented at the University of New South Wales by Green et al. in 1983 and was patented in 1985 [54]. The development of BC solar cells evolved as a process simplification from high efficiency processing based on microelectronics and was motivated by the fabrication of high efficiency solar cells applying low cost technologies. Therefore the emphasis during the development of BC solar cells was on the establishment of simple and low cost processes and techniques which were suitable for large area solar cells and for mass production. In contrast to high efficiency solar cells of its time the resulting processing sequence requires no photolithography, no expensive anti reflection coatings and avoids the use of an expensive metallization scheme.

The main advantages of BC solar cells are smaller contact widths of the finger metallization compared to conventional screen printing. Smaller finger widths allow for closer finger spacing, which is important for emitters with a high sheet resistance of around 100 Ω/sq. Based on the laser grooves the metallization reaches a higher aspect ratio (ratio of finger depth to width) which results in an excellent finger conductivity. Relatively simple and reliable realization of a selective emitter structure even in an industrial environment was achieved consisting of an entire shallow emitter diffusion and a heavy diffused emitter underneath the metal contacts. This structure results in a low contact resistance and contact recombination of the finger metallization. A selective metal deposition is applied based on electro-less plating.

In 1985 BP Solar licensed the BC solar cell technology. The scope of the subsequent development work was wide ranging and included different methods and materials for the following key steps in cell production: Grooving of the silicon, *pn* junction formation, dielectric surface passivation, rear surface treatment and metallization. The result was the solar cell structure given in Figure 5.

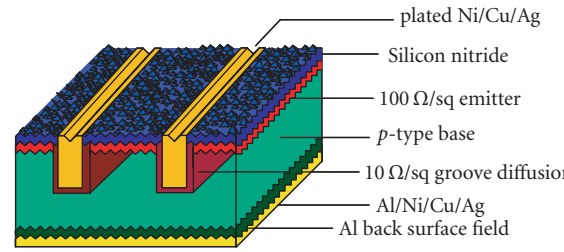


Figure 5: Schematic drawing of a buried contact solar cell.

Table 3: Inferred fabrication steps for BC solar cells of BP Solar.

(1)	Saw damage removal, texture and cleaning of *p*-type silicon wafer
(2)	P_2O_5 deposition on front side
(3)	CVD silicon nitride deposition onto front side
(4)	Laser groove
(5)	Groove damage etch and cleaning
(6)	Heavy $POCl_3$ phosphorus diffusion and shallow P_2O_5 co-diffusion
(7)	Al evaporation to the rear
(8)	Rear contact diffusion
(9)	Electroless plating of Ni
(10)	Sintering
(11)	Etching
(12)	Electroless plating of Cu and Ag
(13)	Laser edge isolation
(14)	IV measurement and sorting

The front grid pattern is fabricated by laser grooving cutting 20 μm wide and 30 μm deep into the surface of the silicon using a high speed, pulsed Nd-YAG laser [55, 56]. For the formation of the emitter a P_2O_5 film is applied as the dopant source for the active silicon surface, whilst $POCl_3$ vapor is used to dope the exposed silicon in the grooves. In this way, the surface is lightly doped for optimum current collection over the entire solar spectrum, whilst the groove regions are more heavily doped for low grid resistance characteristics and metal junction formation. The resulting sheet resistance of the *n*-type surface and groove region is 100 Ω/sq and 10 Ω/sq, respectively [56]. The rear surface of the cell is coated with a thin film of Al using vacuum deposition followed by a high temperature sintering process. The cometallization of the front and rear surfaces is achieved by a sequence of electro-less plating using Ni, Cu and Ag, with intermediate metal sintering. BC solar cells reach in production average efficiencies of about 17%, best solar cells with 18.3% have been demonstrated [57]. According to the descriptions in [55, 58] the following manufacturing process of BC solar cells is summarized in Table 3.

Limitations of the current BC solar cells arise from their thin Al film on the solar cell rear side as described in [58].

Therefore, latest developments are in direction of solar cells with buried contact grid on the solar cell front side and laser fired contacts on the solar cell rear side [56, 59].

5.2. Boron back-surface-field solar cells

Screen-printed Al paste and firing is commonly used for the formation of the BSF. A major drawback of this technology is wafer bowing, especially when the wafers become thinner. Furthermore, the passivation quality of the Al BSF is limited by the recombination rate of alloyed Al on Si. Another dopant candidate for the BSF formation on *p*-type silicon is boron. A boron BSF has a better surface passivation and avoids wafer bowing. However, the application of boron is technologically more difficult. Boron diffusion out of the gas phase needs additional processing steps to reach a BSF only on the cell rear side. Therefore a one-sided fabrication process was developed by Siemens Solar [60] using one-sided boron coating on the rear side and a subsequent boron drive-in at an elevated temperatures. An advantage of the boron BSF solar cell is that the additional process steps for the application of the boron BSF could be implemented in an unchanged remaining process sequence for conventional screen-printed solar cells. A low surface reflection was reached by the combination of a surface texture with an additional silicon nitride anti reflection coating. For the emitter formation a conventional phosphorus gas diffusion using $POCl_3$ is used. For the metallization conventional Ag screen printing on the front and rear sides of the cells is applied. With this process an efficiency improvement of over 10% relative is achieved.

The boron BSF process was implemented into mass production and around 60 MW_p/a were produced at Siemens Solar and their succeeding companies Shell Solar and SolarWorld. Table 4 and Figure 6 show the main solar cell fabrication steps and a schematic drawing of this type of solar cell, respectively.

For further improvements in efficiency a selective emitter structure was developed. With respect to retain cost effective screen printing, a locally highly doped emitter below the screen-printed contacts was developed. Applying the shallow emitter technology to boron BSF solar cells an average cell efficiency of 18.4% was reached on more than 500 cells, the best solar cell had an efficiency of 18.8% [61]. These selective emitter solar cells exhibit a high red response due to the boron back surface field and an almost constant blue response due to the shallow light receiving emitter. The red response could be even improved by the application of a light reflection layer on the solar cell rear side, for example evaporated Al, to enhance the solar cell rear side reflection.

5.3. Heterojunction with intrinsic thin layer solar cells

Sanyo developed the HIT solar cell combining amorphous silicon and monocrystalline silicon [13]. This approach was very successful and Sanyo achieved a total area solar cell efficiency of over 20% [62]. The high efficiency is derived from the excellent passivation ability of the HIT structure on monocrystalline silicon. The non-doped amorphous silicon

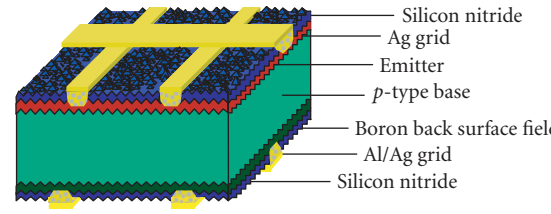


Figure 6: Schematic drawing of a boron BSF solar cell of SolarWorld.

Table 4: Fabrication steps for boron BSF solar cells by SolarWorld.

(1)	Saw damage removal, texture and cleaning of *p*-type silicon wafer
(2)	Boron coating
(3)	Boron drive-in
(4)	Boron glass removal
(5)	Phosphorus diffusion
(6)	Phosphorus glass removal
(7)	Edge isolation
(8)	Silicon nitride deposition
(9)	Screen printing front side
(10)	Screen printing rear side
(11)	Firing
(12)	IV measurement and sorting

(*i*-type a-Si:H) film is sandwiched between *p*-type a-Si:H and the *n*-type monocrystalline silicon wafer on the solar cell front side forming the heterojunction emitter. A further improvement in efficiency was reached by implementing a BSF formed from an *i*-type a-Si:H film sandwiched between *n*-type a-Si:H and the *n*-type monocrystalline silicon wafer on the solar cell rear side.

In production [62] a very thin *i*-type a-Si:H layer and a *p*-type a-Si:H layer with a total thickness of about 10 nm are deposited by plasma CVD on the front of a textured *n*-type solar grade Czochralski monocrystalline silicon wafer of about 1 Ωcm and of about 200 μm thickness. Another very thin *i*-type a-Si:H layer and an *n*-type a-Si:H layer with a total thickness of about 20 nm are deposited at the rear side of the wafer. A transparent conductive oxide TCO is formed on each side of the wafer using sputtering. Ag electrodes are formed on the two wafer sides with a silkscreen printing method. All processes are performed at temperatures below 200°C. There is no need of photo-masking or processing cycles at temperatures as high as 1000°C that might cause thermal damage to the wafer. Besides, the symmetry of the HIT structure also allows solar electricity generation when the solar cell is illumi nated from the rear side. In summary, the inferred solar cell fabrication steps as described in [62] are given in Table 5. Figure 7 shows a schematic drawing of this type of sollar cell.

Sanyo developed the HIT structure and demonstrated cell efficiencies up to 21.5% [63]. After implementation of the HIT solar cell fabrication process into production the average cell efficiency is estimated to about 18% to 20% according to their module power output. Another feature of the HIT solar cells is its excellent temperature characteristics,

Table 5: Inferred fabrication steps for HIT solar cells produced by Sanyo, according to [62].

(1)	Saw damage removal, texture and cleaning of *n*-type silicon wafer
(2)	Deposition of *i*-type and of *p*-type a-Si:H to the front side
(3)	Deposition of *i*-type and *n*-type a-Si:H to the rear side
(4)	Deposition of TCO to the front side
(5)	Deposition of TCO to the rear side
(6)	Silver silk screen contact print to the front side
(7)	Silver silk screen contact print to the rear side
(8)	Contact sintering
(9)	Contact solder coating
(10)	IV measurement and sorting

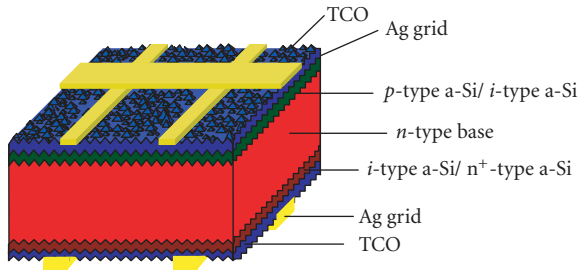


Figure 7: Schematic drawing of a HIT solar cell produced by Sanyo.

better than the temperature dependence of conventional *pn* junction solar cells. This superior temperature dependence results in up to 10% higher module power output at standard test conditions. An efficiency limitation of today's HIT solar cells is obviously in the moderate short circuit current density of around 36 mA/cm^2, possibly due to the transparency of the transparent conductive oxide layer on the solar cell front side.

5.4. Interdigitated back contact solar cells

High efficiency back junction solar cells have a collecting junction only on the solar cell rear surface whereas the front surface is well passivated. The minority carriers, which are mainly generated at the front surface, have to diffuse a long way to the rear junction. Hence, back junction solar cells require a high ratio of bulk diffusion length to cell thickness.

First designs of interdigitated back contact (IBC) solar cells were investigated by Lammert and Schwartz [14]. For the carrier collection and transport, the doped areas and the electrode contacts are alternating (interdigitated arrangement). For the development of high-efficiency IBC solar cells, point contacts were introduced by Sinton et al. [64] to reduce the rear surface recombination. The rather complex manufacturing process in the beginning was simplified by a trench mesa design, which involves only one photolithography step and no alignment steps at all [65]. A first commercialization was carried out by the SunPower Corporation (CA, USA).

Key design features that contribute to high efficiency include localized back contacts with reduced contact recombination losses, a gridless front surface which permits

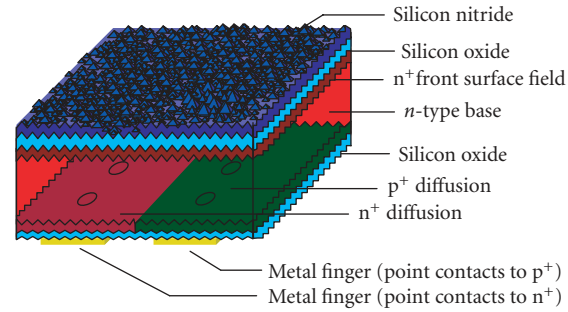


Figure 8: Schematic drawing of an IBC solar cell of SunPower.

optimization of light trapping and passivation, and a backside metallization approach that provides internal rear surface reflection and very low series resistance. Because the minority carriers must diffuse through the entire wafer thickness to reach the collecting junctions at the rear, the IBC solar cell design requires extraordinarily high lifetime silicon starting material. SunPower is using wafers with lifetimes greater than 1millisecond and a thickness of 200 μm [66]. With regard to low-cost processing of the diffusion, the wet etching and the cleaning were adapted to industrial processes. A simple texture process is used for the generation of a random texture on the front side. PECVD silicon nitride deposition is applied. To reduce fabrication cost, the pattern of the rear side for boron and phosphorus diffusion was developed with low-cost screen printing technology to replace photolithography in the fabrication of IBC solar cells [67, 68]. Silicon dioxide is formed on the entire rear side, and a pattern of holes in the oxide at the boron and phosphorus diffused areas is generated. For good light reflectance, aluminum is deposited as first metal layer on the planar silicon dioxide coated rear side and patterned according to the *p*- and *n*-doped regions. For electrical conductivity, the patterned aluminium areas are plated with Ni as a diffusion barrier and to achieve good contact resistance against Cu. The Ni plating is followed by plating of Cu for electrical conductivity and finished by a flash of Ag to protect the Cu. The solar cell fabrication is then completed by an annealing step for the contact formation. As an overview, the IBC solar cell structure is shown in Figure 8 and the inferred solar cell fabrication steps according to [65–67] are given in Table 6. SunPower demonstrated IBC solar cells with efficiencies of 21.5%. In production, the average efficiency is estimated to be over 20%.

Limitations of IBC solar cell fabrication arise from the requirement of silicon wafers with high minority carrier lifetimes, which restricts the silicon quality choice [68], but the wide tolerance on the wafer thickness and resistivity help for tolerable wafer cost [69].

5.5. Emitter wrap through solar cells

The basic idea of emitter wrap through (EWT) solar cells [15] is to leave all metal contacts on the solar cell rear side, but to use a front-side emitter for additional current collection. The electrical interconnection between the front-

Table 6: Inferred fabrication steps for IBC solar cells of Sunpower.

(1)	Saw damage removal and cleaning of *n*-type silicon wafer
(2)	Boron diffusion
(3)	Boron glass removal
(4)	Rear-side SiN_x
(5)	Front-side boron etching
(6)	Oxidation
(7)	Pattern of rear side for phosphorus diffusion
(8)	Rear-side phosphorus diffusion
(9)	Front-side oxide etching and texture
(10)	Front-side phosphorus diffusion
(11)	Diffusion glass removal
(12)	Silicon nitride deposition on front and rear sides
(13)	SiN_x patterning for contact points
(14)	Aluminium sputtering
(15)	Aluminium patterning
(16)	Plating Ni, Cu, Ag
(17)	Annealing
(18)	IV measurement and sorting

side emitter and the rear-side emitter is accomplished by laser-drilled holes which have a heavy phosphorus diffusion and, if possible, are metallized for higher conductivity. The number of holes required for EWT solar cells is in the range of some tens per 1 cm^2. In principal, EWT solar cells are designed similar to IBC solar cells with an additional emitter on the solar cell front side and holes for the connection of the front to the rear-side emitter. Applying sophisticated fabrication processes including photolithography, best cell efficiencies of 21.4% have been reached on a small area of 4 cm^2 and float-zone silicon [70]. Applying industrial process technologies, efficiencies of 16.1% were reported on 100 cm^2 solar cells on Czochralski silicon [71].

With regard to low-cost production, Advent Solar is going to produce EWT solar cells using multicrystalline silicon wafers and conventional industrial solar cell processing [72, 73]. Starting with about 1 Ωcm *p*-type multicrystalline wafers, EWT solar cells are fabricated by laser drilling a 2 mm × 0.75 mm hole grid pattern. The holes are about 60 μm in diameter. The wafer is then etched and cleaned. To achieve low-cost EWT solar cells, it is important to define *n*- and *p*-type regions on the rear side for the emitter and the base contact. A screen-printed glass or dielectric layer is applied by Advent Solar to the wafer base as a diffusion barrier to isolate the *p*- and *n*-type regions and to block locally the diffusion of phosphorus for the separation of *n*- and *p*-metallization regions in EWT solar cells.

The screen-printed diffusion barrier also acts as a barrier to the diffusing species, which are used to form the emitter or the base junction. The phosphorus diffusion barrier has a 0.35 μm wide open channel [72]. Al is later printed and alloyed to compensate the exposed region in the channel. After diffusion, the phosphorus glass is etched off, but the diffusion barrier is not etched off. SiN_x:H is applied on both sides. Al lines are printed over the 0.35 μm channels and Ag lines are printed connecting the holes and sequentially

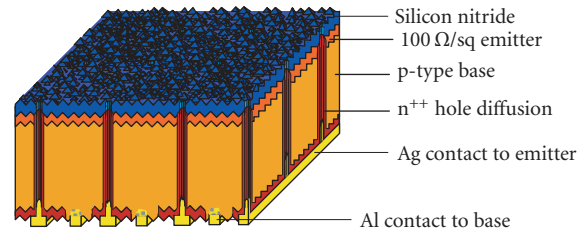


Figure 9: Schematic drawing of an EWT solar cell of Advent Solar.

Table 7: Inferred fabrication steps for EWT solar cells produced by Advent Solar according to [72].

(1)	Laser hole drilling into *p*-type silicon wafer
(2)	Saw damage removal, texture, and cleaning
(3)	Screen printing of diffusion barrier containing an open channel
(4)	Phosphorus diffusion
(5)	Phosphorus glass etching
(6)	Silicon nitride deposition to front and rear sides
(7)	Al printing to *p*-type region in channels
(8)	Ag printing to *n*-region and connecting holes
(9)	Firing
(10)	IV measurement and sorting

fired to form contacts. In this configuration, the diffusion barrier serves to isolate the *p*-metallization and provide a surface passivation on the base. A feature is also that the Al metallization is made wider than the contact width, thus allowing for improved line conductivity. The solar cell fabrication steps according to [72] are given in Table 7 and the solar cell structure is shown in Figure 9.

In production, EWT solar cells with efficiencies of 15.2%, about 600 mV open circuit voltages, 35.4 mA/cm^2 short circuit current densities, and 71.3% fill factors have been reached with screen-printed Ag metallization [72]. With the deposition of an additional solid metal conductor, the seriesresistance could be improved and best EWT solar cell efficiencies of 15.6% together with 600 mV open circuit voltages, 36.3 mA/cm^2 short circuit current densities, and 71.6% fill factors could be reached [73]. A number of standard optimizations, along with the attention to improve the series resistance, are expected to raise the mean EWT cell efficiency to 16% in the near future. Advent Solar offered a 170 W_p module in 2006 in correspondence to the mentioned solar cell parameters.

6. SUMMARY

In 2006, around 86% of all wafer-based silicon solar cells are featuring screen-printed front and rear contacts as well as silicon nitride as the antireflection coating with excellent surface and bulk passivation properties. We look into this dominant solar cell technology and its fundamentals. Currently used processes and equipment for the standard screen-printed solar cell are discussed for all process steps in detail: (i) saw damage removal, texture, and cleaning, (ii) phosphorus diffusion, (iii) phosphorus glass removal and

edge isolation, (iv) silicon nitride deposition, (v) Ag screen printing of the front contact, (vi) Al/Ag screen printing of the rear busbars, (vii) Al screen printing of the rear, (viii) firing, and (ix) IV measurement and sorting. Average solar cell efficiencies of around 15% for multicrystalline and around 16.5% for monocrystalline Czochralski silicon are standard in the industry. The main optical and electrical losses of this technology are discussed. Also, the requirements for a solar cell technology under industrial environment are considered. With regard to higher cell efficiencies, advanced solar cell concepts are studied. To date, only a few of these more advanced technologies were introduced into industrial production having a market share below 15% of all wafer-based silicon solar cells in 2006.

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