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New developments on front-end electronics for the CMS Resistive Plate Chambers

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Abstract

A novel version of the front-end electronics for the CMS Resistive Plate Chambers is described. It is based on a new front-end ASIC, designed and manufactured in the 0.8 μm BiCMOS technology by Austria Mikro Systeme. The main improvements with respect to the previous version (Loddo et al., Proceedings of the Fourth International Workshop on Resistive Plate Chambers and related Detectors, Napoli, 15–16 October 1997) [1] concern the input impedance, the threshold uniformity and the timing performance. Simulation and test results will be shown, together with a brief description of the automatic test system for both front-end chip and board.

1. Introduction

The Resistive Plate Chambers (RPC) are gaseous parallel-plate detectors that will be used in the CMS experiment for the muon trigger system [2]. The RPC proposed for CMS consists of two 2 mm gaps with common pick-up readout strips in the middle and will be operated in the so-called avalanche mode, for sustaining event rates up to 1000 Hz/cm^2. The shape of the current signal, induced by a single cluster, is described by the function $I(t) = I_0 \exp(t/\tau)$, $0 \le t \le 15$ ns, for freon-based gas mixtures having electron drift speed in the order of 130 μm/ns and τ (gas time constant) ~ 1 ns at the nominal working point of the detector. The expected dynamic range is between 20 fC and 20 pC.

In the barrel RPC, the readout strips are 1.3 m long, while their width ranges between 2 and 4 cm, according to RPC position in the apparatus. The characteristic resistance of the strip ranges from 40 to 15 Ω, respectively, while their capacitance ranges between ~ 160 and ~ 420 pF. The induced signal has a rise time (~ 1 ns) shorter than propagation delay of the strip, therefore this one behaves like a transmission line and must be properly terminated at both ends, in order to avoid reflections. The

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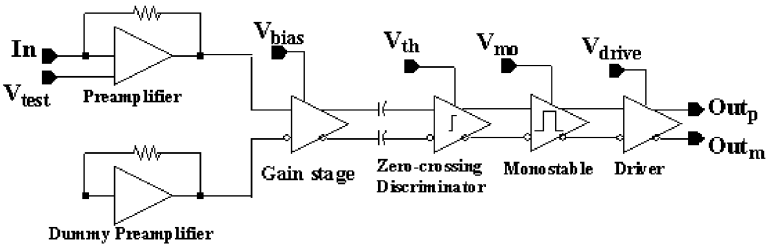

Fig. 1. Single-channel block diagram.

strip is terminated on one end by the input resistance of preamplifier, on the other end by a resistor.

2. Circuit description

The circuit is made of eight identical channels, each one consisting of amplifier, zero-crossing discriminator, monostable and differential line driver. A single channel block diagram is shown in Fig. 1. Since the termination resistor has a small and variable value, an AC coupling between strip and amplifier is required. The required power supplies are +5 V and GND, while the overall power consumption is about 45 mW/channel.

2.1. The amplifier

The preamplifier (Fig. 2) is a cascoded common emitter transimpedance stage, with input impedance of 15 Ω at the signal frequencies (between 100 and 200 MHz), in order to match the characteristic impedance of the strip in the worst case of 4 cm wide strips. In the other cases, the matching will be obtained adding an external series resistor at board level. The current in the input transistor $Q_{\rm in}$ is about 700 μA and, in order to reduce the supply voltage value [3], a resistor $R_{\rm casc}$ is added between the emitter and the base of the cascode transistor $Q_{\rm casc}$. The value of $R_{\rm casc}$ is about 4.5 kΩ which is much higher than the input impedance of $Q_{\rm casc}$ and only a small fraction of the signal current is lost into $R_{\rm casc}$. The open-loop gain is about 100, while the dominant pole is about 116 MHz and the charge sensitivity is 0.5 mV/fC. A "dummy" input preamplifier was required to balance the DC output variations of the real input first stage.

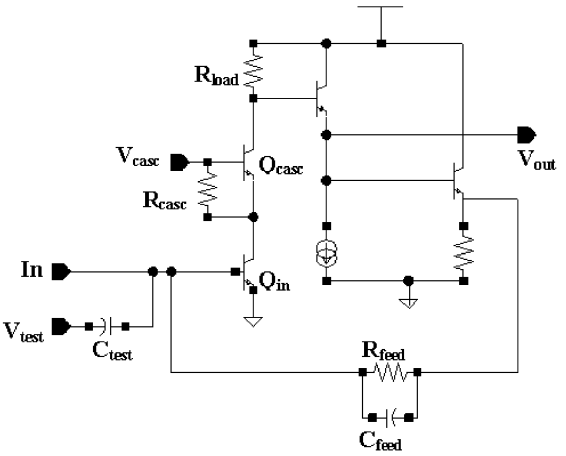

Fig. 2. Current preamplifier.

The expression of the input admittance is

$$Y_i(s) = sC_{\rm in} + \left(\frac{1}{R_{\rm feed}} + sC_{\rm feed}\right)\left(1 + \frac{g_m R_{\rm load}}{1 + sR_{\rm load}C_{\rm load}}\right) \quad (1)$$

where $C_{\rm in}$ is the input capacitance of $Q_{\rm in}$, $R_{\rm feed}$ and $C_{\rm feed}$ are the feedback resistance and capacitance, respectively, $g_m \sim 27$ mA/V is the transconductance; the parallel of $R_{\rm load}$ and $C_{\rm load}$ is the internal load across which the voltage gain is produced.

If we set $R_{\rm load}C_{\rm load} = R_{\rm feed}C_{\rm feed}$ and define $C_{\rm tot} = C_{\rm in} + C_{\rm feed}$ then

$$Y_i(s) = sC_{\rm tot} + \frac{g_m R_{\rm load}}{R_{\rm feed}}. \quad (2)$$

If we impose, $R_{\rm in} = R_{\rm feed}/g_m R_{\rm load} = 15$ Ω then

$$Z_i(s) = \frac{R_{\rm in}}{1 + sR_{\rm in}C_{\rm tot}}. \quad (3)$$

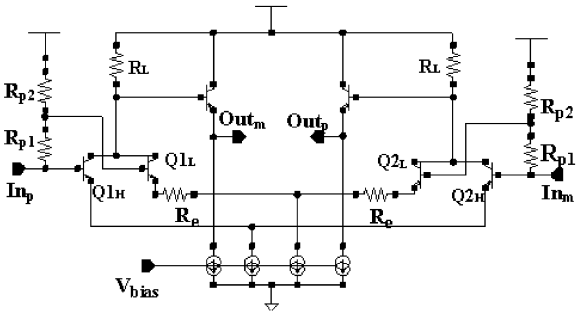

Fig. 3. Gain stage.

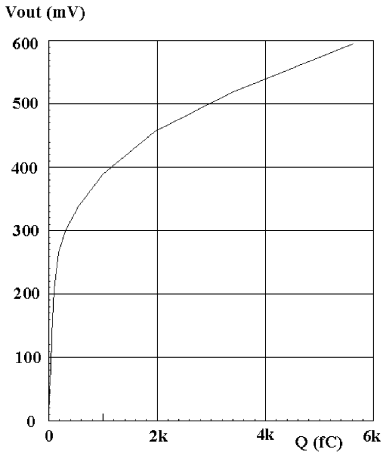

Fig. 4. Transfer characteristics of the amplifier.

Being $C_{tot} < 3$ pF, the pole of the above expression is > 1 GHz and

$$Z_i \sim R_{in} \sim 15\ \Omega \quad (4)$$

up to the signal frequencies (between 100 and 200 MHz), as required by the matching condition.

The preamplifier is DC-coupled to the gain stage, whose schematic is shown in Fig. 3. It is designed to provide non-saturated response on the dynamic range and to fully exploit the zero-crossing timing, as shown in Section 2.3 The circuit must ensure a linear behavior only in the threshold range ($Q_{in} < 100$ fC), while for larger inputs non-linearity is not a problem. A simple way to meet these requirements is to design a two-step piecewise-linear function fitting, which is accomplished by summing the output currents of two gain segments. The preamplifier output is sent to two differential amplifiers having different gains but common output nodes. The external amplifier ($Q1_H$, $Q2_H$, R_L) has a DC voltage gain ~ 7 and is used to amplify small signals ($Q_{in} < 200$ fC) while the internal one ($Q1_L$, $Q2_L$, R_L) has a voltage gain ~ 0.25 and amplifies signals above 200 fC never saturating in the dynamic range. The overall charge sensitivity is 2 mV/fC for input charges < 100 fC and the power consumption of the amplifier, including the "dummy stage", is 15 mW. The transfer characteristics of the amplifier are shown in Fig. 4.

2.2. Noise calculation

The equivalent circuit of RPC and amplifier for noise analysis is shown in Fig. 5 [4].

The parallel noise is dominated by the thermal noise of the terminating resistor R_0 at the far end of the strip and can be represented by an equivalent noise current generator with power density i_n^2 (A^2/Hz) in parallel to R_0:

$$i_n^2 = 4KT/R_0 \sim 1.1 \times 10^{-21}\ A^2/Hz\ (T = 300\ K). \quad (5)$$

The series noise is represented by an equivalent noise voltage generator with power density e_n^2 (V^2/Hz) in series with the input:

$$e_n^2 = 4KT(0.5/g_m + R_{BB'}) \sim 4.9 \times 10^{-19}\ V^2/Hz \quad (6)$$

$R_{BB'} \sim 11\ \Omega$ being the base spread resistance of Q_{in}.

The preamplifier is current sensitive, so it is convenient to transform the noise voltage generator into an equivalent current noise generator with

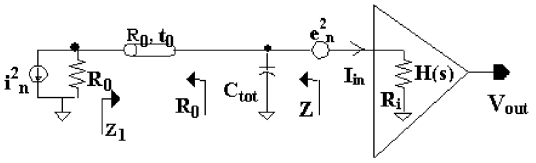

Fig. 5. Equivalent circuit of RPC and amplifier for noise analysis.

power spectrum

$$i_{ns}^2 = \frac{e_n^2}{|R_i + Z|^2} \tag{7}$$

where $Z = R_0/(1 + sR_0C_{tot}) \approx R_0$ is the impedance shown in Fig. 5, assumig the strip impedance matched at the far end. For simplicity, assuming $R_{in} \sim R_0 = 15\ \Omega$, as shown in Eq. (4), we obtain

$$i_{ns}^2 = \frac{e_n^2}{4R_0^2} = 5.5 \times 10^{-22}\ \mathrm{A^2/Hz}. \tag{8}$$

The rms noise at the output is found by the integration of the noise current through R_{in} multiplied by the square of the magnitude of the amplifier transfer function $H(j\omega)$

$$V_{ns} = \sqrt{\int_0^\infty i_{ns}^2 |H(j\omega)|^2\, df} \sim 2.1\,\mathrm{mV\ rms} \tag{9}$$

where

$$H(s) = \frac{V_{out}(s)}{I_{in}(s)} \approx \frac{A}{1 + s\tau_L} \tag{10}$$

with τ_L being the time constant of the dominant pole and A the gain. Assuming the line to be ideal, the impedance seen at the far end is

$$Z_1(s) = R_0 \frac{Z_i(s) + R_0 \tanh(st_0)}{R_0 + Z_i(s)\tanh(st_0)} \tag{11}$$

with $t_0 \sim 7$ ns being the propagation delay and Z_i the expression (3). Then, the parallel noise current flowing into the preamplifier is

$$i_{np}^2 = i_n^2 \left| \frac{R_0}{R_0 + Z_1} \right|^2. \tag{12}$$

If we assume again $Z_i = R_{in} = R_0$, then $Z_1 = R_0$ and

$$i_{np}^2 = \frac{i_n^2}{4} = 2.8 \times 10^{-22}\ \mathrm{A^2/Hz}. \tag{13}$$

The rms parallel noise at the output is

$$V_{np} = \sqrt{\int_0^\infty i_{np}^2 |H(j\omega)|^2\, df} \sim 1.5\ \mathrm{mV\ rms}. \tag{14}$$

Finally, the total output noise is

$$V_n = \sqrt{V_{ns}^2 + V_{np}^2} \sim 2.6\ \mathrm{mV\ rms}. \tag{15}$$

Simulations of the circuit, including all the noise sources, show a total output noise ~ 3.4 mV, corresponding to an ENC ~ 1.7 fC, fully satisfying the noise limit of 4 fC.

2.3. Zero-crossing discriminator

Accurate timing information from the RPC is crucial for unambiguous assignment of the event to the related bunch crossing. The simplest method to provide trigger pulse is the leading edge timing, which can be performed by a threshold discriminator. Though simple, this method is affected by the amplitude time-walk. In the case of RPC signals, with a 1000:1 dynamic range (20 fC–20 pC), the time walk is ~ 10 ns [1].

An amplitude-independent timing response can be approximated by the technique of zero-crossing: a CR network differentiates the input signal and produces a bipolar pulse crossing the zero in correspondence of the peak of the input signal [5]. In the hypothesis that input signals have the same peaking time, the zero-crossing time is independent of signal amplitude and can be used as time reference. This solution can be easily integrated into ICs. In Fig. 6, the block diagram of the implemented discriminator is shown. The differential outputs of the amplifier are strongly differentiated through a CR network having 4 ns time constant. This grants the fast recovery time of the baseline, which is < 50 ns even in the case of a 20 pC input charge.

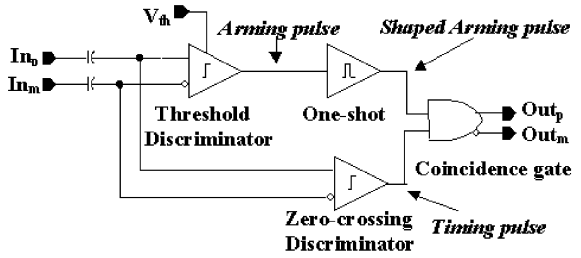

Fig. 6. Discriminator block diagram.

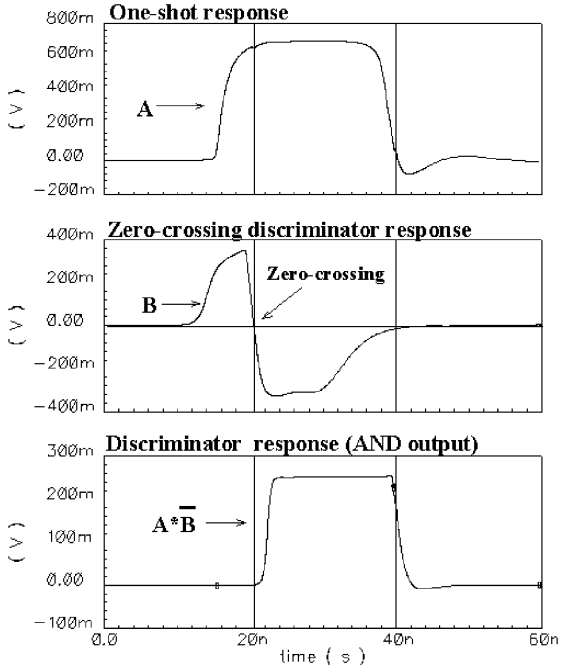

Fig. 7. Discriminator principles of operations.

The threshold (arming) discriminator provides charge selection capability and consists of a double stage differential amplifier, with a threshold range between 5 and 500 fC. A one-shot circuit follows the arming discriminator. It shapes the arming pulse typically at 20 ns, in order to ensure its coincidence with the Zero-Crossing Discriminator (ZCD) output.

The ZCD is another double-stage differential amplifier, having no threshold. Combining the output of the one-shot and that of the ZCD, we obtain the output of the discriminator, as shown in Fig. 7. The power consumption of the discriminator is about 8 mW.

2.4. The monostable and the output driver

In a RPC working in avalanche mode, an afterpulse often accompanies the avalanche pulse with a delay ranging from 0 to some tens of ns. Therefore, a monostable circuit follows the discriminator and gives a pulse shaped typically at 100 ns, in order to mask the possible second trigger and to prevent the ZCD from triggering on the noise. The choice of the pulse length comes from the trade-off between the possible second trigger and the dead time. The expected maximum rate being less then 400 kHz/channel, a length of 100 ns, giving a dead time of 4%, has been considered a good compromise. In any case, there is a possibility to tune it in the range 50–300 ns. The dead time introduced by the monostable is ~ 10 ns and its power consumption is ~ 2 mW.

The Output Differential Driver is capable to feed a twisted pair cable with a signal level of 250 mV on 100 Ω, as required by LVDS receivers. The power consumption is ~ 18 mW but the driver output current could be tuned in order to compensate process variations.

3. Test results

Fifteen untested prototypes were received and tested in April 1999. One chip did not work at all, while on the others, the gain of the amplifiers was set to the nominal value of 2 mV/fC. The gain uniformity inside each group of four channels driven by the same control input resulted to be less than $\pm 7\%$, i.e., setting the threshold to the nominal value of 20 fC, the maximum expected error was only ± 1.5 fC. Noise measurements were performed after the insertion of 15 Ω termination resistors at the inputs. The ENC resulted to be around 1.8 fC, as foreseen by the simulations.

3.1. Timing performance

Timing performances were measured using an oscilloscope HP54542C. The threshold was set to 30 fC and charge pulses ranging between 35 fC and 20 pC were injected by means of a pulse generator LeCroy 9210. For all the prototypes, the maximum input to output propagation delay dispersion among the eight channels as a function of the input charge overdrive was measured, as shown in Fig. 8. With the exception of two chips, one having a $\Delta T \sim 5$ ns and the other one with a $\Delta T \sim 0.9$ ns and therefore not acceptable, all other chips show a ΔT typically less than 0.5 ns. Fig. 9 shows the average delay time vs. the charge overdrive: for

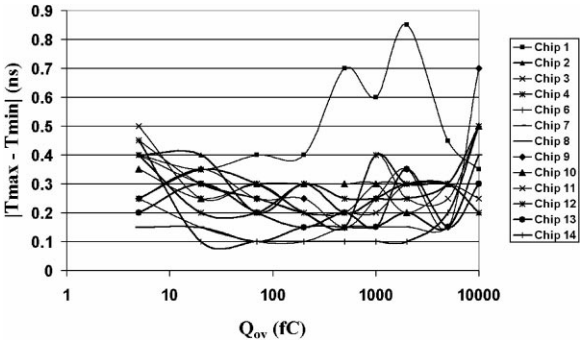

Fig. 8. In-chip delay dispersion.

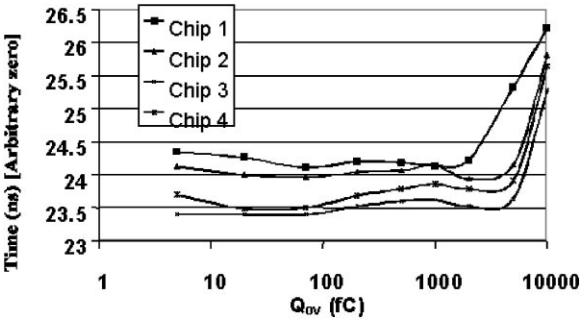

Fig. 9. Timing response vs. charge overdrive.

$Q_{ov} < 5$ pC, the time walk is less than 0.6 ns. For bigger charges, up to 20 pC, it rises up to few ns, but the probability of occurrence of such pulses is less than 10% and not significant for trigger purposes.

3.2. Irradiation test

A preliminary irradiation test was performed to study the effects of the total absorbed dose on the chip performance. One board was irradiated in the Bari Gamma Irradiation Facility and the total dose was about 1.3 Gy, corresponding to 10 LHC years in the barrel. Another board was tested at the LENA Reactor, in Pavia. In this case, the total dose was ~ 24 Gy of gamma and fast neutrons. The results are encouraging, because neither permanent damage nor significant variations in the chip performance were observed. Further tests for Single Event Upset evaluation are under preparation.

4. Chip characterization

RPC trigger needs precise timing evaluation but, due to process parameters variations, chips belonging to different silicon wafers could provide different time responses. The goal is to house two chips with the same propagation delay onto each FEB and this requires a precise chip characterization.

A FEC test board equipped with four test sockets and some control logic has been built and tested. The board is controlled by a PC instrumented with the following National Instruments data acquisition boards:

- 6024E Family Multifunction I/O, 12-bit resolution, 200 kS/s and 20 MHz counter/timer with 24-bit resolution;
- 6507 Family PCI-DIO-96, 96 TTL lines of parallel digital I/O;
- PCI-GPIB interfaces, NI-488.2M.

The instrumentation is completed by a Scope and a Pulse Generator (PG). A detailed block diagram of the test bench is shown in Fig. 10.

4.1. Operation flow

The acquisition program, developed with LabView 5.1, consists of the following steps:

(1) The PG is set in burst mode via GPIB, and the signal out characteristics are set (for example 50 fC at 10 kHz);
(2) using 5 bits of the DIO96 port, chip and channel are selected;
(3) a threshold value is set;
(4) the gain control voltage is set to the nominal value of 2.5 V;
(5) the GATE signal is sent to the PG and, during this time, the pulses coming from the PG and those from the electronics output are counted;
(6) the n_{PG} countings from PG and the n_{chip} from chip are compared, and the gain value is automatically increased or decreased until $n_{chip}/n_{PG} = 0.5$;
(7) after this calibration phase, the delay propagation time for the eight channels/chip is measured with a TDC having a 30 ps time resolution for 100 ns full-scale time range.

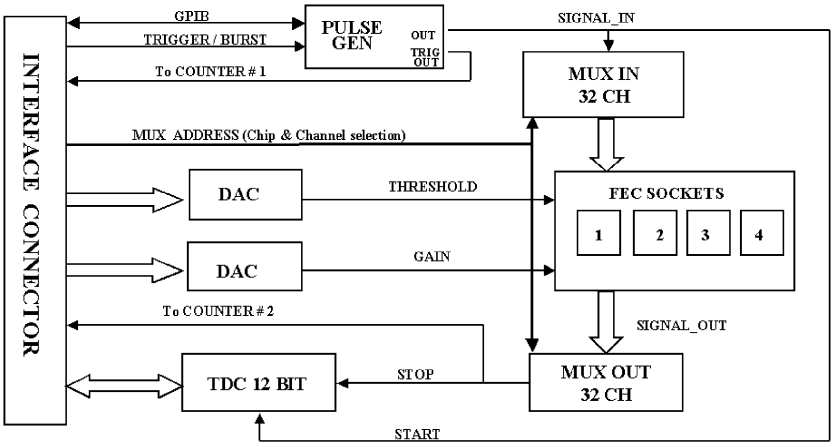

Fig. 10. FEC test bench block diagram.

The maximum spread among the eight channels must be less than about 0.5 ns, otherwise the chip is discarded. If the condition is met, the average delay value is assumed as the "chip propagation time".

The same set-up can be used to verify the full functionality of the FEBs, once the chips have been mounted on and before the installation on the chambers. The power supplies and the functionality of the threshold Digital to Analog Converters will be checked over the full dynamic range. Then, the amplifier gains will be set, together with the width and the height of the output pulses. Finally, the delay time of the two chips will be measured to verify the uniformity of the chip behavior.

5. Conclusions

A BiCMOS front-end chip for the CMS–RPC detectors has been designed and prototyped. Measurements on 14 prototypes agree with the simulation results and fulfil all the design constraints. Also preliminary irradiation tests are satisfactory, even if other tests are required to fully characterise the chip. Moreover, an accurate test procedure for the final production of front-end chip and board has been developed and succesfully tested.

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