CMS Conference Report

24 January 1997

Radiation Effects on Breakdown Characteristics of Multiguarded Devices

M. Da Rold, A. Paccagnella, A. Da Re, N. Bacchetta, A. Candelori and D. Bisello

INFN, Sezione di Padova and Università di Padova

G. Verzellesi, G.-F. Dalla Betta and G. Soncini

Università di Trento

R. Wheadon

INFN, Sezione di Pisa

Abstract

Multiguard structures are used in order to enhance the breakdown voltage of microstrip detectors. In this work we studied the electrical properties of devices designed in four different layouts on n-Si substrates, based on a central diode surrounded by various p^+ and/or n^+ floating rings. In particular we measured the main DC characteristics and we compared the experimental results with those simulated by a two-dimensional drift-diffusion computer model. Device noise was also measured for the central diode as a function of the applied voltage. We repeated all measurements after neutron and gamma irradiation, in view of the application of these devices to silicon microstrip detectors for future high energy physics experiments. For example at the LHC the level of radiation damage expected during the detector lifetime implies very high bias voltages for the detector operation. Multiguards can offer a solution, provided the optimisation of the design takes into account the radiation effects.

Presented at the IEEE *Nuclear Science Symposium*, Anaheim 3-9 november 1996

Submitted to IEEE Trans. on Nucl. Sc.

Radiation Effects on Breakdown Characteristics of Multiguarded Devices

M. Da Rold[a,b], A. Paccagnella[b,c], A. Da Re[c], G. Verzellesi[d], N. Bacchetta[b], R. Wheadon[e], G.-F. Dalla Betta[d], A. Candelori[b,c], G. Soncini[d,f] and D. Bisello[a,b]

[a] Università di Padova, Dipartimento di Fisica, Via Marzolo 8, I-35131 Padova, Italy

[b] INFN, Sezione di Padova, Via Marzolo 8, I-35131 Padova, Italy

[c] Università di Padova, Dipartimento di Elettronica e Informatica, Via Gradenigo 6a, I-35131 Padova, Italy

[d] Università di Trento, Dipartimento di Ingegneria dei Materiali, Via Mesiano 77, I-38050 Trento, Italy

[e] INFN, Sezione di Pisa, Via Livornese 1291, I-56010 San Piero a Grado, Pisa, Italy

[f] IRST, I-38050 Panté di Povo, Trento, Italy

Abstract

Multiguard structures are used in order to enhance the breakdown voltage of microstrip detectors. In this work we studied the electrical properties of devices designed in four different layouts on n-Si substrates, based on a central diode surrounded by various p^+ and/or n^+ floating rings. In particular we measured the main DC characteristics and we compared the experimental results with those simulated by a two-dimensional drift-diffusion computer model. Device noise was also measured for the central diode as a function of the applied voltage. We repeated all measurements after neutron and gamma irradiation, in view of the application of these devices to silicon microstrip detectors for future high energy physics experiments. For example at the LHC the level of radiation damage expected during the detector lifetime implies very high bias voltages for the detector operation. Multiguards can offer a solution, provided the optimisation of the design takes into account the radiation effects.

I. INTRODUCTION

When a high reverse bias is applied to a p^+-n junction, high fields may occur locally, leading to impact ionisation and avalanche multiplication. Due to the junction curvature, the space charge region (SCR) also extends laterally. At the surface, the electron accumulation layer underneath the passivation oxide may prevent this extension, and the applied voltage drops across a shorter distance. Therefore high fields are most likely to occur close to the Si-SiO_2 interface. Many solutions have been studied in order to control the electric field at the surface [1]. Among them is the multiguard structure, which consists of a series of floating guard rings around the main junction (diode). When the reverse bias is applied to the junction, its SCR also spreads laterally and, when the voltage is high enough, it reaches that of the innermost floating guard, establishing punch-through conduction between guard and main junction. At a higher applied voltage, more guards are reached by the diode SCR. Thus, at the surface the potential drops across a longer distance [1][2][3]. To the purpose of avoiding any increase of the reverse current and noise associated to the breakdown phenomena, the structure design must be well balanced to limit the field strength in the depleted region and to prevent the SCR from reaching the device edges. Here surface generation occurs and excess leakage can be drawn to the junction via punch-through conduction across the guards[4].

The multiguard structure can offer a reliable solution to the breakdown problem in silicon microstrip detectors foreseen in future experiments at the LHC. Here the harsh radiation environment causes the substrate type inversion after a few years of runs at full luminosity, and high voltages might be needed to fully deplete the detector [5][6]. Provided that the design optimisation takes care of the effects induced by the radiation, multiguards can also guarantee stability in the detector performances versus the environmental instabilities (humidity, mobile ions, contaminants, etc.).

In this paper we present a full characterisation of the multiguard structure from an experimental point of view and with the aid of device simulations (Sec.II.). The effects of ionising radiation (Sec.III.) and neutron induced bulk damage (Sec.IV.) have been studied.

II. DEVICE CHARACTERISATION

The devices we studied are diodes produced at CSEM (Neuchatel-Switzerland) on $300\,\mu m$ thick n-type silicon wafers. The backside is uniformly n^+ implanted and metallised to create the ohmic contact. The substrate is available for two resistivity values: high resistivity, i.e. $\rho = 10 k\Omega cm$ ($N_{eff} \sim 4 \times 10^{11} cm^{-3}$) and low resistivity, i.e. $\rho = 2.5 k\Omega cm$ ($N_{eff} \sim 2 \times 10^{12} cm^{-3}$). On the junction side, each device consists of a 5×5 mm^2 p^+ implant surrounded by a large p^+ guard (100 μm wide). Other floating p^+ and/or n^+ guards surround the diode. The distance between each pair of adjacent concentric guards (G1,..,G6) increases moving from the centre to the edge of the device. They are designed in four different layouts as sketched in Fig.1: L1 (6 p^+ guards), L2 (6 p^+ guards and field plates), L3 (6 p^+ guards with n^+ isolation) and L4 (6 n^+ guards). All the guards have a metal connection to allow probing, while the silicon surface is SiO_2 passivated. We tested all four devices for each of the eight available wafers: five high resistivity and three low resistivity. All measurements were performed in air at room temperature. Humidity was not controlled.

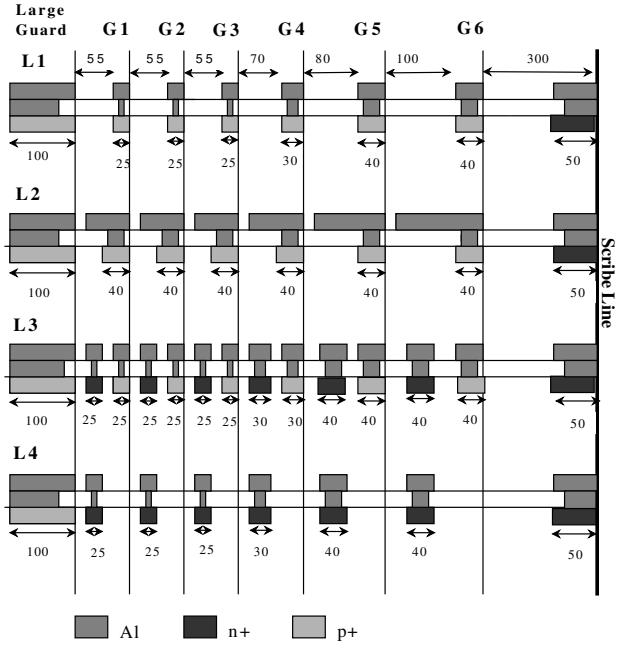

Fig. 1 Cross section of the multiguard structure for the four layouts: L1, L2, L3 and L4. Distances are expressed in μm. The main junction is on the left, while the edge is on the right. The guard labels are specified along the top.

A. I-V Characteristics

In Fig.2 the I-V curves are shown for an L2 diode and for a diode without the floating guards. In these measurements the diode and large guard were both grounded while a positive voltage was applied to the backside. The diode and the large-guard currents were both measured. A current compliance was set in order to avoid excess junction heating. In the diode without multiguards the breakdown occurs on the large-guard at 300V, while the diode current remains stable at higher voltages, until a compliance occuring on the guard current stops the measurement. In the L2 multiguard structure the breakdown occurs on the guard at 620V, while the diode current is stable up to 700V.

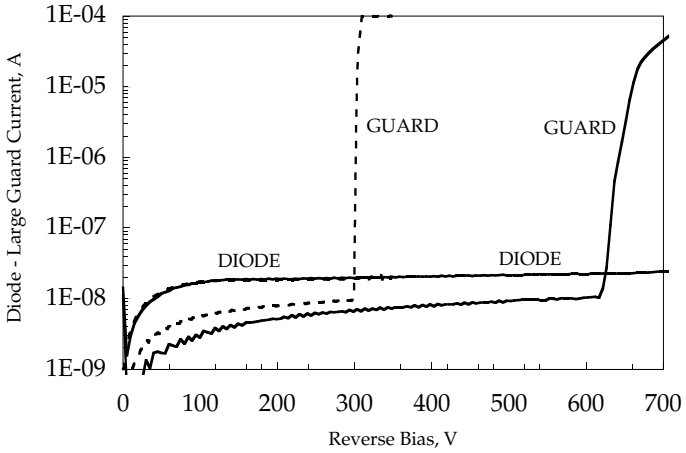

Fig. 2 I-V characteristics for a devices L2 (solid) and a diode without multiguard (dotted), both the diode and the large-guard currents are plotted. The substrate has low resistivity.

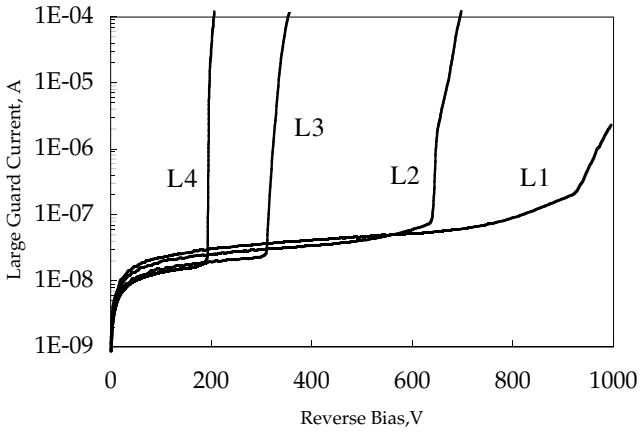

Fig. 3 I-V characteristics for all the devices with multiguards from the same wafer at high resistivity. Only the large-guard currents are plotted.

In Fig.3 the large-guard I-V curves are shown for all the layouts from the same high resistivity wafer. Regarding L1, the current increases considerably over 900V. In all wafers we measured a breakdown voltage over 800V and up to more than 1000V. For L2 there is an abrupt current raise at 650V. The breakdown voltages for all L2 devices fall in the range 520V-700V. L3 breaks down at around 300V in all high resistivity samples; in low resitivity devices this limit falls to 250V. L4 shows a breakdown voltage of about 200V in all devices. In most devices, when the large-guard current increases sharply, the breakdown does not occur simultaneously on the central diode, except for L4, which shows diode breakdown at the same voltage as the large-guard. In some structures we measured an increase of the diode current at low voltages. This will be discussed in section C.

From the I-V characteristics of all available devices we noticed that the breakdown voltage is layout dependent and the design is not always optimised to increase the breakdown limit over the performance given by the unguarded diode.

B. Voltage Distribution

In Fig.4 the guard voltages are plotted against the applied bias for an L2 device.

A positive voltage was applied to the backside, while the diode and the large-guard were kept grounded. At low applied bias, the voltage on the guards follows the bulk potential. At around 15V the voltage curve for the first floating guard bends and a potential difference with the backside appears. Due to the applied voltage, the diode and large-guard SCR also extends laterally. At low bias no potential is applied to the floating guards which are practically shorted to the bulk. When the bias is high enough for punch-through to occur between the grounded junctions and the first floating guard [7], it is reached by the diode and large guard SCR and it starts to exhibit a potential difference to the backside. From the same picture it is clear how only the first guards are reached by the SCR and show a potential difference to the bulk in the entire bias range considered. This implies that the outermost guards are not in punch-through with the active area and we can exclude that

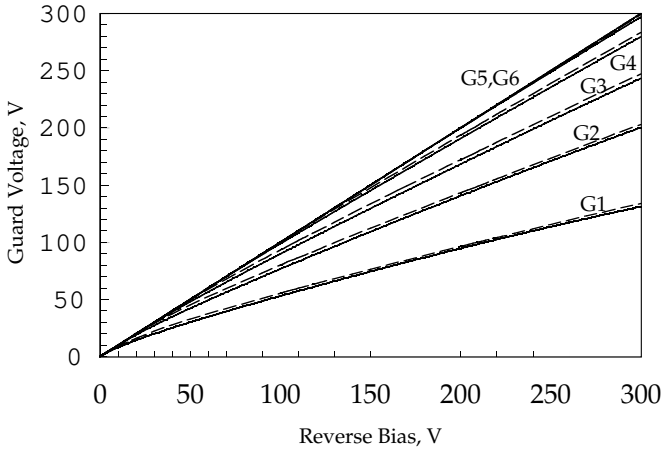

Fig. 4 Guard Voltages vs Reverse Bias for an L2 device at high resistivity. The experimental curves are solid, while the simulated ones are dashed.

current is drawn from the edge, at least up to 300V.

The dashed lines in Fig.4 are simulation results. These were obtained by means of the 2-D device-analysis program DESSIS, included in the T-CAD software package by ISE AG [8]. DESSIS solves Poisson's and carrier continuity equations, with electron- and hole-current densities given by the drift-diffusion model. All main physical effects of interest in device modelling are supported. In our simulations, carrier mobilities are functions of doping concentration and both longitudinal and transverse components of the electric field. Carrier lifetimes are functions of the doping concentration. A fixed positive charge density of 2.5×10^{11} cm^{-2} has been placed at the Si-SiO_2 interface, where a midgap surface-state distribution with a surface-recombination velocity of 10^3 cm/s (corresponding to a surface-state density of 10^{11} cm^{-2}, given a capture cross section of 10^{-15} cm^2) has been included, as well. Impact ionisation is modelled according to [9].

As can be seen in Fig.4, the overall agreement between simulation and experimental curves is satisfactory. In particular, the most relevant simulation outcome, i.e. the onset of punch-through between different guard rings, is predicted quite accurately. The slight quantitative discrepancies are to be ascribed to the uncertainties on the actual doping distribution and oxide charge density.

The two-dimensional electric potential distributions across the bulk silicon are shown in Fig.5 and Fig.6 for an L2 device at $V_{bias} = 10V$ and $V_{bias} = 70V$, respectively. These curves were obtained by simulations, considering a negative voltage applied to the diode and large-guard and keeping the backside at ground. They refer only to the large-guard (LG) and the two first floating guards, G1 and G2, which are specified along the top of the figure. Also the SiO_2 surface is indicated along the top of the figures. At $V_{bias} = 10V$ the zero potential line crosses the device underneath the gap between the first and second floating guard. Here only the first guard is in punch-through with the main junctions and the SCR does not reach G2. This is more clear in Fig.7, showing the hole density distribution . A hole path exsists between G1 and LG. At $V_{bias} = 70V$ the zero potential line is far beyond the second guard which is in punch-

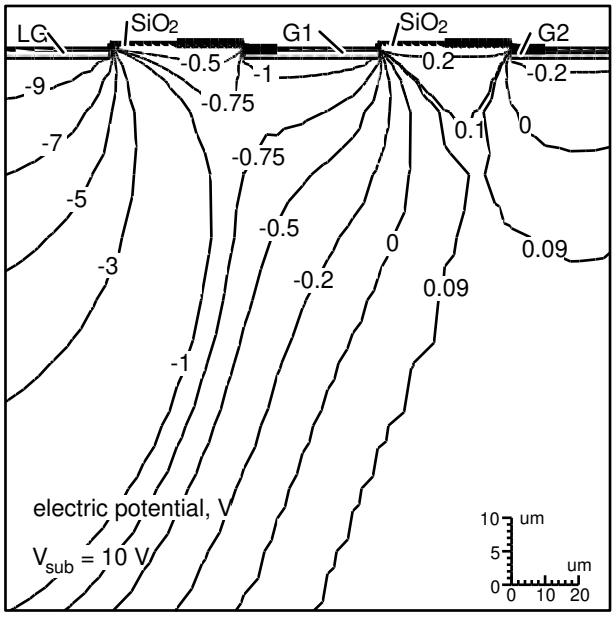

Fig. 5 Two-dimensional electric potential distribution in the region between large-guard (LG) and two floating guards (G1, G2) for an L2 device at $V_{bias} = 10V$

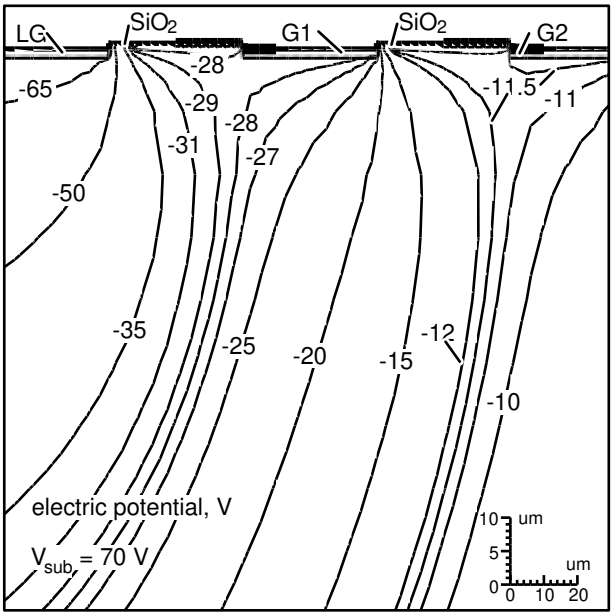

Fig. 6 Two-dimensional electric potential distribution in the region between the large-guard (LG) and the two first floating guards (G1, G2) for an L2 device at $V_{bias} = 70V$.

through with G1. A hole path is now visible also between G2 and G1 (Fig.8). This lies well below the SiO_2-Si interface. In Fig.5 most of the potential drops between the large-guard and G1. In particular the potential lines are quite dense close to the large-guard, between the junction and the accumulation layer. Here high fields are present, and when they are above the critical value they can lead to avalanche breakdown.

We compared the experimental and simulated curves for all the layouts. Devices L2 and L3 showed a good reproducibility, i.e. the curves from different wafers were exactly overlapping. Also the agreement between experimental and simulated curves

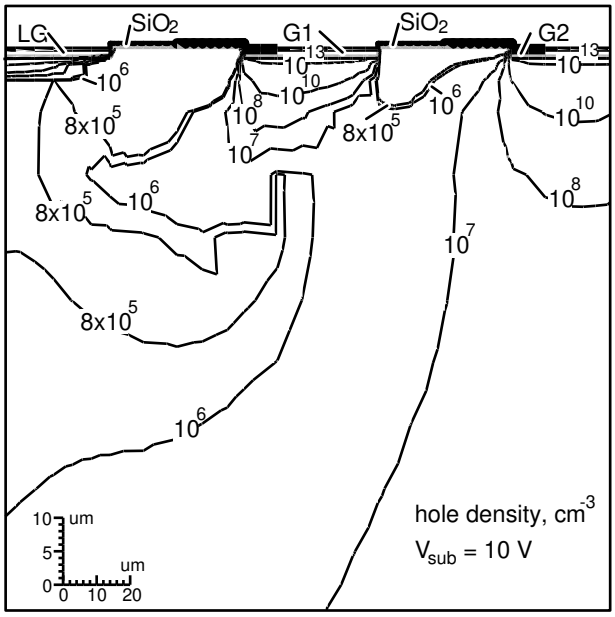

Fig. 7 Two-dimensional hole density distribution in the region between the large-guard (LG) and the two first floating guards (G1, G2) for an L2 device at $V_{bias} = 10V$.

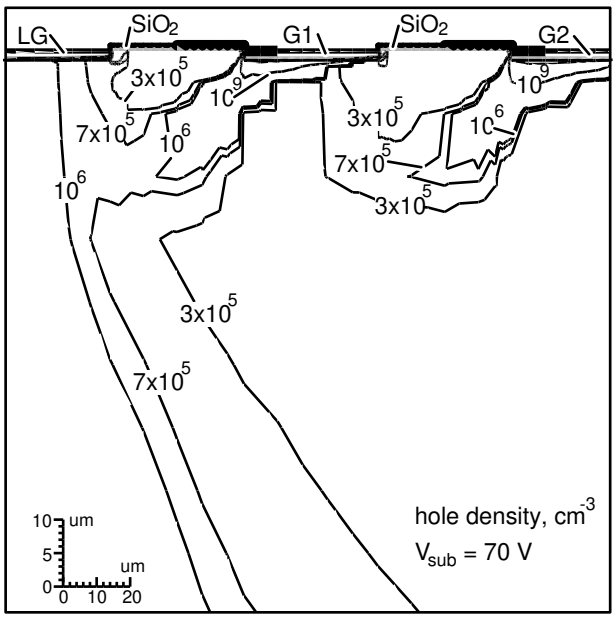

Fig. 8 Two-dimensional hole density distribution in the region between the large-guard (LG) and the two first floating guards (G1, G2) for an L2 device at $V_{bias} = 70V$.

was very good. The same cannot be stated for L1. In this case the curves from the various wafers showed significant variations. A possible explanation is that in L2 and L3 field plates and n^+ guards set the surface potential at a fixed value, with the result of a decreased sensitivity to oxide inhomogeneities. On the other hand the voltage distribution for L1 is more sensitive to the oxide and the environmental conditions and the agreement with simulations is not so good.

In devices L3 the n^+ guards are found to be at the same potential as the adjacent external p^+ guards. The punch-through current flows from the external edges towards the active area, in this way the p^+-n-n^+ junction of two following guards is forward biased by a small current, with a resulting negligible potential drop. This is confirmed by the electron/hole distributions obtained by simulations.

The devices with a breakdown below 300V are L3 and L4. L4 has only n^+ floating guards which are shorted to the backside through the n-type bulk. Therefore the applied potential drops entirely across the $15\mu m$ separating the p^+ and n^+ implants, and avalanche occurs when its value is around 200V. This value is in agreement with that proposed by [1] for the breakdown voltage of a p^+-n-n^+ punch-through:

$$V_{BD} = \epsilon_c W_{gap} - \frac{1}{2}\frac{qN_D W_{gap}^2}{\epsilon_s} \quad (1)$$

where W_{gap} is the base width of the punch-through diode, in our case the gap between the p^+ and n^+ implants, q, the electron charge, N_D, the substrate donor density, ϵ_s, the silicon dielectric constant and ϵ_c the critical field given by [1]:

$$\epsilon_c = 4010 N_D^{1/8} \quad (2)$$

.

Considering a gap width of $15\mu m$ and an average doping density $N_D = 10^{12} cm^{-3}$ we obtain $V_{BD} \sim 190V$, which is close to the breakdown value of 200V we measured. Possible discrepancies can be due to the fact that equation 1 is obtained for a one-dimensional devices: no curvature effect is taken into account.

When avalanche ocurred in the L3 devices (at $\sim 300V$) we measured on the first n^+ guard, which is $15\mu m$ from the large-guard, a voltage of 200V. Therefore avalanche occurs between the large-guard and the first n^+ floating guard.

C. Noise Behaviour

In Fig.9 the RMS-noise characteristics as a function of the applied bias is shown together with the I-V curves for an L3 device. We measured the RMS noise at the output of a PreShape32, low noise charge amplifier, designed in the RD20 collaboration[10]. The signal from the diode was decoupled through a 200pF capacitor, while the diode was grounded through a $1M\Omega$ resistor and the large-guard directly grounded. When the current breakdown occurs, a corresponding noise increase above the shot noise level is expected. In the case of L3, even if the diode current was stable, we measured an increase in the RMS noise level corresponding to the breakdown on the guard. This is due to the capacitive coupling between the large-guard and the diode.

In some devices (Fig.10) we measured a current increase on the diode at low voltages. This is not as abrupt as an avalanche breakdown, but, as expected, it leads to an increase of the RMS noise that follows the square root of the leakage current. Over 320V the square root dependence is lost and the abrupt noise increase can be due to microdischarge phenomena [11]. The low voltage current increases have been seen in some devices. They are not layout dependent and are randomly distributed among devices from different wafers. We attribute them to processing inhomogeneities.

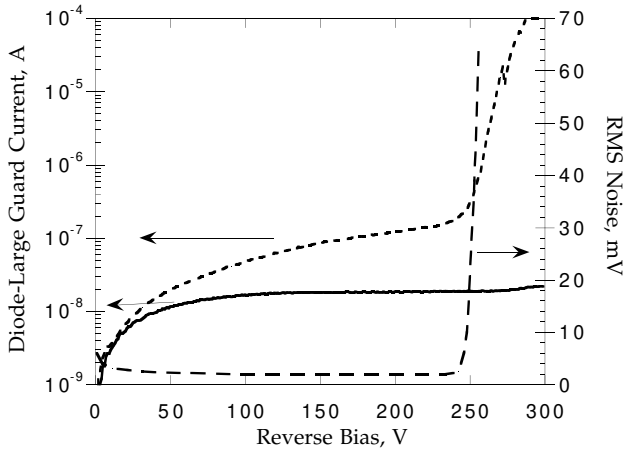

Fig. 9 Diode (solid) and large-guard (dotted) current together with the noise curve (dashed) for an L3 device, low resistivity.

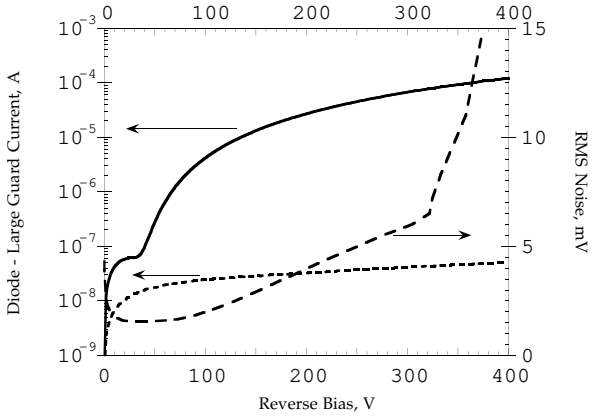

Fig. 10 Diode (solid) and large-guard current (dotted) together with the noise curve (dashed) for a L1 device showing low voltage breakdown on the diode. The substrate is high resistivity.

It is important to point out that measuring the signal amplifier output by means of an oscilloscope, we observed current spikes randomly distributed in time at voltages below the breakdown. These ones are rare and as the RMS meter integrates the signal over a relatively long time, they do not bring any contribution to the RMS level. Therefore the RMS measurement must be considered mainly a qualitative technique which can give information on breakdown phenomena, but not very sensitive to discharges occuring rarely in time which can lead to signal degradation also at voltages below the breakdown point.

III. GAMMA IRRADIATION

A. *Effects on breakdown*

We irradiated three multiguard devices, L1 (high resistivity), L2 and L3 (low resistivity) and two unguarded diodes (low resistivity) in a ^{60}Co gamma cell at the CNR-FRAE laboratory in Bologna for a total dose of 200krad(Si) received in 40 minutes. Irradiations were performed in air at room temperature in a humidity controlled environment. All the diodes where kept reverse biased at 220V during irradiation. In these conditions the junction was reverse biased well above full depletion and close to the breakdown voltage for the L3 device. In the diodes the potential drop across the passivation oxide is not generally controlled by the junction bias, unless the guards are provided with field plates. It is likely that the radiation induced oxide charge build up is not uniform in different points of the same device and between different layouts [12].

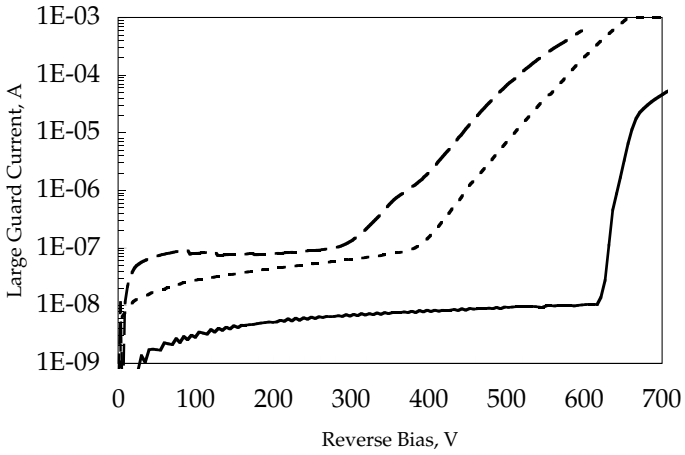

Fig. 11 I-V for a gamma irradiated (dose= 200krad) L2 device, low resistivity. The characteristics refer to the large-guard: before irradiation (solid), soon after irradiation (dashed) and four days after irradiation(dotted).

The I-V characteristics of an L2 device before and after irradiation are shown in Fig.11. Right after irradiation a decrease of the breakdown voltage by more than 300V was measured, while after four days a 100V recovery was recorded. The current increase at breakdown after irradiation is in this case less abrupt than in unirradiated devices. The radiation induced changes are less evident for L3, where the breakdown voltage is only 50V lower immediately after irradiation and it recovers completely after a 18 day annealing at room temperature. The breakdown voltage in device L1 is 200V, while it was 900V before irradiation. The current raise is very smooth as in the case of L2. These breakdown values are consistent with noise measurements, which show the diode noise abrupt increases at the guard breakdown.

At voltages below the breakdown we measured a high leakage, more than one order of magnitude higher than before irradiation for the L2 device. The large-guard collects all the current from the depletion region due to the multiguards. This region is quite superficial and it is possible that the surface leakage dominates over the bulk leakage. The enhanced leakage may then be due to the surface damage. This enhancement depends on the layout: more evident for L2 and L1 (around one order of magnitude) and less for L3 and the unguarded diode (around 2-3 times). Moreover in all the devices the diode leakage is two times higher. Here we suppose that the bulk contribution is dominating.

B. *Voltage Distribution*

The guard voltage curves for L2 are shown in Fig.12. The potential difference between guards and central diode is increased after irradiation, expecially for the inner guards. This

trend appears also on the curves for L1, where the differencies between the guard voltages before and after irradiation is even larger. In device L3 there is no difference between the curves before and after irradiation. In this case the surface potential is mainly determined by the n^+ guards between the p^+ ones and the oxide influence is minimal.

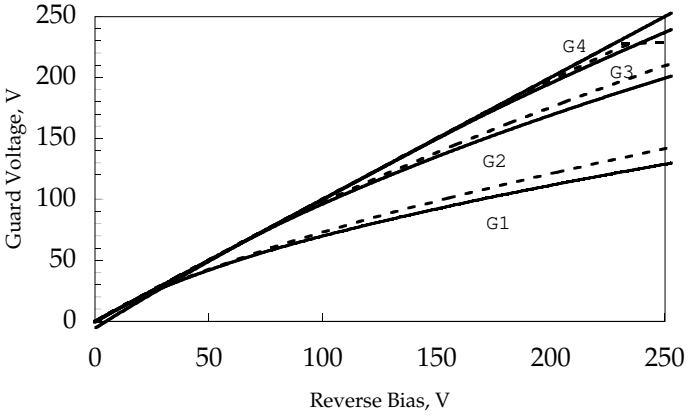

Fig. 12 Guard Voltage distribution before (solid) and after gamma irradiation (dotted), dose 200krad, for a L2 device, low resistivity.

The effect of the gamma irradiation on the voltage distribution along the guards is less dramatic than that observed for the breakdown voltage. The guard potential is determined by the onset of punch-through. This is mainly a bulk conduction phenomenon occuring in a p^+-n-p^+ double junction and its threshold is only weakly affected by changes in the accumulation layer at the silicon surface [7] which is increased by the radiation induced oxide damage. On the other hand the surface field distribution can be heavily modified by the enhanced electron accumulation. Therefore fields above the critical value for avalanche can occur locally and the breakdown voltage is lowered.

IV. NEUTRON IRRADIATION

Two devices L1 (p^+) and L3 (p^+ and n^+), on a high resistivity substrate, were irradiated at the Lena Reactor, Pavia. The nominal neutron fluence was $10^{14} n/cm^2$, achieved in an irradiation time of only a few minutes at room temperature. The neutron energy spectrum was peaked at $2MeV$. Three weeks after irradiation we performed the first set of measurements. From C-V measurements we found that $V_{dep} = 50V$, while before irradiation it was around $30V$. This increase in the depletion voltage can be explained by substrate inversion to an effective p-type, due to radiation induced deep levels [6][5]. The I-V characteristics are shown in Fig.13. The current level at 100V (over depletion) is 200 μA on the diode and 50 μA on the large-guard and it exponentially increases in both cases with the reverse bias, up to 600V. Here both the diode and guard currents increase more rapidly and at 650V the measurements stopped due the onset of a current compliance at 2mA. Considering a leakage damage constant of $3.5 \times 10^{-17} A/cm$ [6] and the irradiation fluence, we would have expected a leakage increase of about 30 μA due to the diode volume only.

Fig.14 shows the guard voltages after neutron irradiation. All the guards show a potential difference with the bulk also

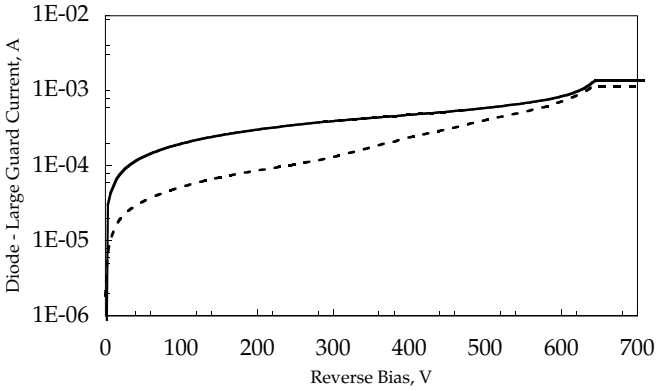

Fig. 13 I-V characteristics for a L3 device, high resistivity, three weeks after neutron irradiation, $\Phi = 10^{14} n/cm^2$. The solid line is the diode current, the dotted line is the large guard current.

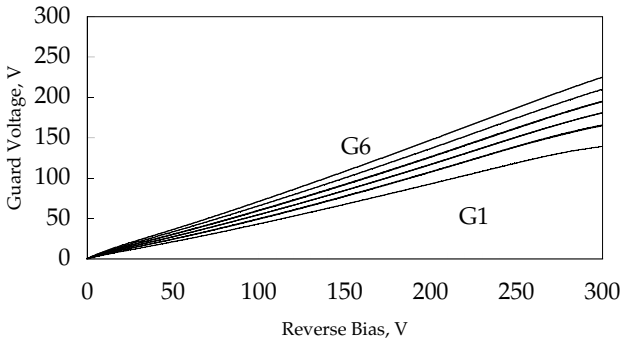

Fig. 14 Guard Voltage for a L3 device, high resistivity, three weeks after neutron irradiation, $\Phi = 10^{14} n/cm^2$.

at low bias. The guard voltages increase almost linearly with the applied voltage. The punch-through mechanism responsible for the guard self bias(Fig.4) is not detectable anymore and the guards seem to be connected by a series resistance. This may be due to the substrate type inversion. Due to the inversion, the guards at the surface may not be isolated anymore and the same resistive path between them could draw current from the device edge to the diode. This may explain the enhanced leakage current we measured. Moreover the layout dependence measured before irradiation was almost completely lost after irradiation, as the curves for L1 and L3 show the same behaviour.

After five months (Fig.15) V_{dep} was between 150 and 180 V. This increase is due to room temperature anti-annealing [6], resulting in a enhanced p-type effective concentration. It is difficult to measure exactly the doping concentration as the C-V curves are found to be frequency dependent, due to charged states responding at different frequencies. Moreover the high leakage current can affect the measurement. Therefore the value given for the depletion voltage is only indicative of the modification in the substrate during the time. In Fig.15 the leakage is still very high and a bending of the curve is visible at around 280V. Again the layout dependence is weak. Comparing the results obtained three weeks after irradiation and five months afterwards, we saw that the diode current was

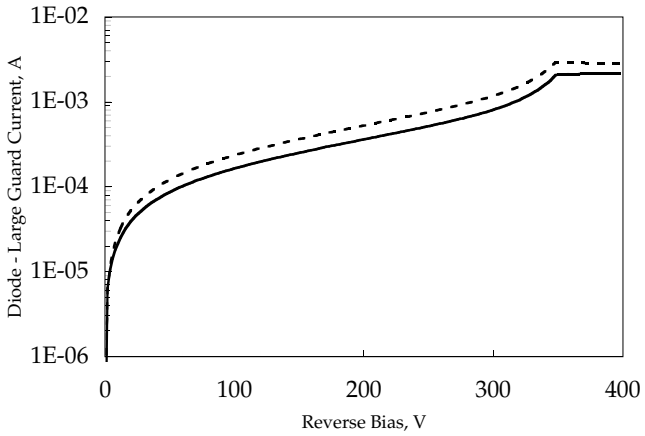

Fig. 15 I-V characteristics for a L3 device, high resistivity, five months after neutron irradiation, $\Phi = 10^{14} n/cm^2$. The solid line is the diode current, the dotted line is the large guard current.

the same. Therefore no annealing was observed. On the other hand, the large-guard current is much higher five months after irradiation, even higher than the diode current. As we discussed, after inversion the diode and the large-guard are not isolated anymore from the device edges and a stronger contribution to the leakage from the surface generation is likely to occurr. This is even more evident after a period of anti-annealing which causes the increase in the effective p-type concentration. In this case the central junction is more effectively connected to the device edge.

V. CONCLUSIONS

Multiguard structures can increase the breakdown limit of a diode, provided they are carefully designed. Layouts L1 and L2 have high breakdown voltages, while the L3 devices have a low voltage limit. In these devices, avalanche occurs in the region between the large-guard and the first n^+ floating guard. This happens to be too close to the central junction: according to Baliga's model [1], a gap twice as wide could improve the breakdown voltage a few hundred volts. In most devices the current breakdown occurs only on the large-guard. Nevertheless this must be avoided as it leads to an increase in the diode noise level.

The device simulations have proved to reproduce the device behaviour quite well. This tool can be employed to improve the multiguard design as the presence of high field regions, where avalanche may occur, can be foreseen.

After gamma irradiation at 200krad(Si), the voltage distribution along the guards does not change dramatically, while the electric field distribution at the silicon surface produces current breakdown at lower voltages. Layout L3 seems to be the least affected by radiation induced damage: the surface potential is mainly controlled by the n^+ guards, therefore it is not very sensitive to the increase of oxide/interface charges. Nevetheless its performance before irradiation was quite poor compared to L1 and L2. After irradiation the breakdown voltages for all the devices are comparable.

After neutron irradiation at a fluence above the silicon inversion point, the guard self bias is not determined anymore by punch-through. As a result a conductive path connects the guards to the device edges and excess leakage can be drained to the diode, leading to an increase in the reverse current.

VI. ACKNOWLEDGEMENTS

We would like to acknowledge Dr. P.G. Fuochi and Dr. M. Lavalle from the CNR-FRAE Institute for their kind support with gamma irradiations. We also thank prof. P. Benetti, from Pavia University, for his friendly availability for neutron irradiations.

VII. REFERENCES

[1] B.J. Baliga, Modern Power Devices, New York: John Whiley & Sons, 1987, pp. 62-100.

[2] L. Evensen, A. Hanneborg, B. Sundby Avset and M. Nese, "Guard ring design for high voltage operation of silicon detectors", *Nucl. Instr. and Meth. in Phys. Res.*, vol. A 337, pp 44-52, July 1993.

[3] A. Bishoff, N. Findeis, D. Hauff, P. Holl, J. Kemmer, P. Klein, P. Lechner, G. Lutz, R.H. Richter and L. Strüder, "Breakdown protection and long-term stabilisation for Si-detectors", *Nuclear. Instr. and Meth. in Phys. Res.*, vol. A326, pp. 27-27, 1993.

[4] D. Bisello, M. Da Rold, L. Franzin, A. Paccagnella, R. Wheadon, " Radiation Effects on Breakdown in Silicon Multiguarded Diodes", *Il Nuovo Cimento*, vol 109 A, n.9, pp. 1343-1350, Sept. 1996.

[5] A. Chilingarov, H. Feick, E. Fretwurst, G. Lindström, S. Roe, T. Shulz, "Radiation studies and operational projections for silicon in the ATLAS inner detector", *Nucl. Instr. and Meth. in Phys. Res*, vol. A360, pp. 432-437, 1995.

[6] F. Lemeilleur, S.J. Bates, A. Chilingarov, C. Furetta, M. Glaser, E.H.M Heijne, P. Jarron, C. Leroy, C. Soave, I. Trigger, "Study of characteristics of silicon detectors irradiated with 24 GeV/c protons between -20°C and $+20^{\circ}$C", *Nucl. Instr. and Meth. in Phys. Res.*, vol A360, pp. 438-444, 1995.

[7] A. Paccagnella, D. Bisello, M. Da Rold, Yu. Gotra, and P. Benetti, "Study of Punch-Through Characteristics in Irradiated MOSFETs", *IEEE Trans. Nucl. Sci.*, vol. 41, no.6, pp. 2511-2520, December 1994.

[8] ISE Integrated Systems Engineering AG, Modeling of semiconductor technology, devices, and systems, Reference Manual, 1994.

[9] R. Van Overstraeten and H. De Man, "Measurements of the ionization rates in diffused silicon p-n junctions", *Solid St. Electr.*, vol. 13, pp. 583-608, 1970.

[10] M. Raymond, L. Jones, RD20 PreShape32 User Manual, CERN/RD20

[11] T. Ohsugi, Y. Iwata, H. Ohyama, T. Ohmoto, M. Okada, M. Yoshikawa, N. Tamura, T. Hatakenaka, Y. Unno, T, Kohriki, N. Ujiie, H. Miyata, T. Aso, R. Takashima, A. Murakami, S. Kobayashi, K. Yamamoto, K. Yamamura, M. Muramatsu, "Microdischarges of Ac-coupled silicon strip sensors", *Nucl. Instr. and Meth. in Phys. Res.*, vol. A342, pp. 22-26, 1994.

[12] T.P. Ma, P.V. Dressendorfer, Ionizing Radiation Effects in Mos Devices and Circuits, New York: John Wiley & Sons, 1989, pp. 149-232.