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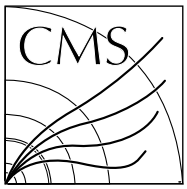

The Compact Muon Solenoid Experiment

CMS Note

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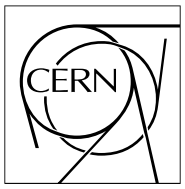

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Test of the Inner Tracker Silicon Microstrip Modules

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Abstract

The inner portion of the CMS microstrip Tracker consists of 3540 silicon detector modules; its construction has been under full responsibility of seven INFN (Istituto Nazionale di Fisica Nucleare) and University laboratories in Italy. In this note procedures and strategies, which were developed and perfected to qualify the Tracker Inner Barrel and Inner Disks modules for installation, are described. In particular the tests required to select highly reliable detector modules are illustrated and a summary of the results from the full Inner Tracker module test is presented.

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1 Introduction

The silicon detector module is a fundamental building block of the CMS Silicon Strip Tracker (SST) [1], [2]: for this reason the module test activity program aimed at selecting extremely high quality detectors, with a number of defects on strips and corresponding readout channels not greater than 2%. The SST covers a radius from 0.2 m to 1.2 m around the beam axis and a total length of 5.6 m along the beam axis. It is subdivided in four main subdetectors: Tracker Inner Barrel and Inner Disks (TIB and TID), Tracker Outer Barrel (TOB) and Tracker End Caps (TEC), for a total of 15148 silicon strip modules. The TIB and the TOB are arranged in coaxial cylindrical layers (4 for TIB and 6 for TOB), while the TID and the TEC are arranged in disks. There are 9 TEC disks on each side of the TOB and 3 TID disks on each side of the TIB. Each TID disk is made of three rings of modules, while TEC disks have from four to seven rings depending on the disk position. In this paper we illustrate the tests and procedures regarding TIB and TID only.

Each test step has been implemented and optimized in order to spot production problems and possibly systematic component weaknesses as early as possible. Because of the specifics of the mechanical construction of the inner barrel and inner disks, it was difficult and risky to replace the modules once they were integrated onto the final mechanical structures. Thus it was important to minimize the replacements of modules found defective after integration, due to defects not directly related to the integration operation. For this reason the test procedures to qualify each Inner Tracker (IT) module were very demanding in terms of defect finding efficiency and overall reliability. The output of the tests was stored on disk and immediately analysed with dedicated ROOT [3] macros which were used to qualify the modules and to give a fast feed-back on the overall production quality. The test data, archived on mass storage devices, were then analysed more deeply by a custom software package able to identify and tag most common strip or channel problems. This code also allowed for the insertion of the main module characteristics and measurement results into the CMS Tracker Construction Database (DB) for permanent storage [4]. The modules which passed the qualification procedure were ready for installation on final substructures which were half-cylinders (also referred to as shells) for the inner barrel, and disks for the inner end-cap regions.

The TIB and TID silicon microstrip modules are described in [1]; to satisfy the needs of the Inner Tracker, the production centres had to build a total number of 3540 (plus spares) single-sided modules (subdivided in 2724 TIB and 816 TID modules) of eleven different types, four for TIB and seven for TID.

A detector module consists of a silicon sensor, a carbon fibre support frame and a hybrid circuit housing the front-end electronics (plus pitch adapter and Kapton circuit). The main production steps were the assembly and the microbonding. In the assembly stage the hybrid and the silicon sensor were glued onto the carbon fibre support frame at an automatic positioning and glueing machine (gantry station) [5]. In the microbonding stage the silicon detector backside (n-side) was bonded to the high voltage line, then bonds were made between the strip AC pads on the p-side and the glass pitch adapter (PA), which had been previously glued on the hybrid and microbonded to the front-end pre-amplifiers. In the TIB/TID INFN community there were two gantry centres (Bari and Perugia) and six bonding centres (Bari, Catania, Florence, Padua, Pisa, Turin) dedicated to module production and testing. After assembly, modules were shipped from gantry centres to bonding centres for final bonding and full testing. The entire testing and bonding process, as well as the gantry process, was done in a clean and humidity controlled environment: all the clean rooms in the INFN laboratories are class 100000 or better. All the modules had to pass a test just after the bonding operations, and a "Long Term" (LT) test later on. The LT aimed at detecting defects or failures which may develop during the initial period of operation (so-called early mortality) and at validating the module performance at both room and low temperatures, similar to the ones foreseen for the Tracker operation at LHC. After each test stage, the percentage of each module defective channels had to stay below 1% (for "Grade A" modules) and between 1% and 2% (for "Grade B" modules, to be regarded as second choice during integration).

Two different test set-ups have been used: the ARC (APV25 Readout Controller) [6] and the LT system [7]. The former is used to rapidly but deeply test single modules at different stages of the production chain; the latter is a more complex system used to continuously readout a batch of up to ten modules while thermal stresses, which emulate the real CMS Tracker operating conditions, are being applied.

All the test procedures and hardware equipment have been discussed and agreed on within the CMS Module Test Working Group (MTWG), which was a working group specifically dedicated to study issues relevant to module test for the whole Tracker, during the entire period of Tracker construction.

In Section 2 a description of the module and its electronics is given. The definitions of the possible module defects are introduced in Section 3, and the description of measurements to be done on modules is reported in Section 4. The hardware equipment used to perform the module test is described in Section 5. In Section 6 the full module test sequence is listed. The tests performed at gantry centres are summarized in Section 7. Tests and procedures used at bonding centres and module selection criteria are presented in Section 8, along with examples of results and the module grading explanation. Section 9 contains a summary of global results derived from the data stored in the Tracker DB; conclusions are in Section 10.

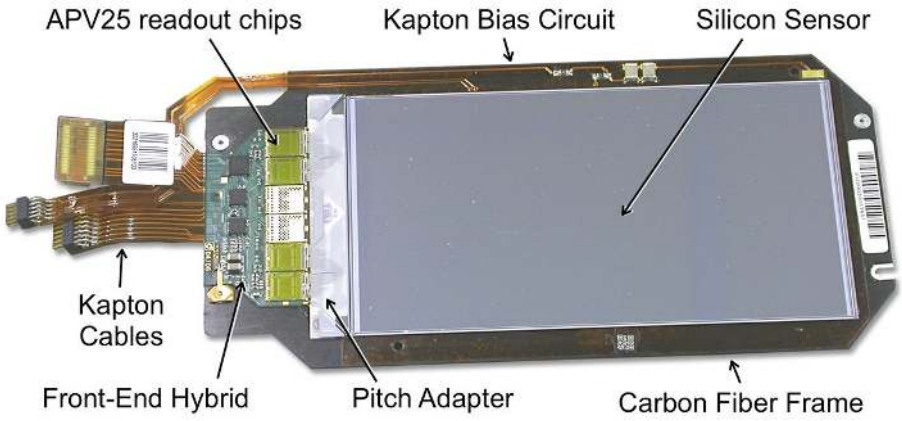

Figure 1: Sketch of a TIB module with its components.

2 Inner Tracker Detector Modules and Front-end Electronics

The detector module design has been kept as simple as possible to ease module mass production and integration. A sketch of a TIB module along with its components is shown in Fig. 1. The sensor, consisting of a 320 μm thick silicon crystal, is glued on a carbon fibre support frame, which also carries the front-end electronics hybrid circuit. The detectors are single-sided n-type, with 512 (or 768) p+ implant strips which are connected to a bias ring via polysilicon resistors (1.5$\pm$0.5 MΩ). The sensors are processed on low resistivity bulk silicon, for improved radiation hardness, with $<100>$ crystal orientation. The aluminium readout strips are AC coupled to the underlying p+ strips by means of thin layers of SiO_2 and Si_3N_4. A detailed description of the silicon sensors can be found in [8]. Modules for Inner Barrel Layers 3 and 4 (L3, L4) have 512 strips with 120 μm pitch, while modules for Layers 1 and 2 (L1, L2), which are the innermost ones, have 768 strips with 80 μm pitch for a higher position measurement resolution. An L3 module mounted on an aluminium test plate is shown in Fig. 2. For the same motivation as in the Barrel region, modules for Inner Disks Ring 1 and Ring 2 (R1, R2) have 768 strips, and modules for Ring 3 (R3) have 512 strips.

The readout chip channel pitch (44 μm), the same for all module types, is matched to the sensor pitch via wire bonding on a glass substrate fanout circuit (pitch adapter). The front-end chips and the ancillary electronics are housed on a hybrid circuit, shown in Fig. 3, realized using kapton multilayer technology. The same hybrid design has been used in the whole TIB and TID, leaving the two central front-end chip locations empty on the hybrids to be mounted on 512 strips modules.

The signals coming from each strip are processed by custom front-end readout chips, named APV25 [9], mounted on the front edge of the hybrid circuit, next to the pitch adapter. The APV25 is a 128 channel chip built in radiation hard 0.25 μm CMOS technology; it requires 2.5V and 1.25V power supply rails. Each channel consists

Figure 2: TIB Layer 3 module mounted on the aluminium test plate and connected to interface cards.

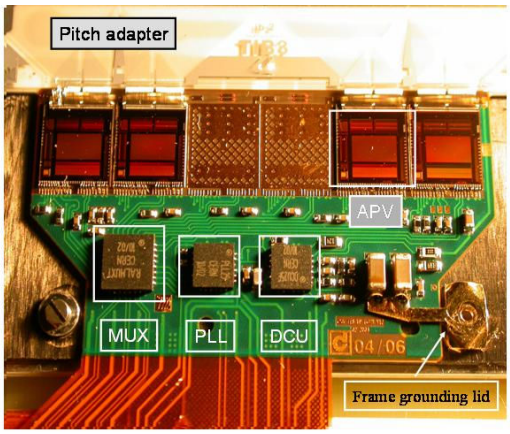

Figure 3: TIB Layer 3 hybrid circuit, with central APV25 locations empty.

of a pre-amplifier coupled to a shaping amplifier which produces a 50 ns CR-RC pulse shape. The shaper output of each channel is sampled at 40 MHz and stored into a 192 cell deep pipeline. The pipeline depth allows for a programmable level-one trigger latency of up to 4 μs, with 32 locations reserved for buffering events awaiting readout. Each pipeline channel is read out by an analogue circuitry which can operate in *Peak* or *Deconvolution* readout mode. In peak mode only one sample per channel is read (timed to be at the peak of the analogue pulse shape). In deconvolution mode [10] three samples are sequentially read and the output is a weighted sum of all three. The deconvolution operation results in a re-shaping of the analogue pulse shape to one that peaks at 25 ns and returns rapidly to the baseline. The deconvolution mode is particularly important for the correct bunch crossing identification during the high luminosity running phase of the LHC. A unity gain inverter is included between the pre-amplifier and the shaper; it can be switched on or off according to experimental needs, the normal operation of CMS Tracker modules being with inverter on. The combination of the readout mode and the inverter status defines four possible APV25 running configurations (Peak Inverter Off, Peak Inverter On, Deconvolution Inverter Off and Deconvolution Inverter On), referred to simply as "modes" in the following. The analogue electrical output signals are converted to analogue light signals and then sent to the DAQ system via optical fibres. The electro-optical conversion circuit (AOH for Analogue Opto Hybrid) is not part of the module test and will not be described.
The hybrid circuit houses three other application-specific integrated circuits (ASIC) which are the DCU, the PLL and the APVMUX. The DCU is the Detector Control Unit [11], monitoring slowly varying parameters on the module, containing ADCs, current sources and an internal temperature sensor. The DCU is used to measure low voltage (LV) levels on the hybrid, high voltage (HV) bias current and temperatures on the module and in the DCU itself. The HV current readings are meaningful only above a few tens of μA, to allow for the appropriate readout range when the silicon sensor has accumulated a substantial fraction of the expected radiation dose. Module temperatures are sensed by two thermistors, the first one sitting on the hybrid itself and the second one on the backside of the silicon sensor. The PLL [12] is a 40-MHz clock and trigger recovery circuit using a self calibration technique. Finally the APVMUX is an interface between the APV25 chip and the optical line driver chip, multiplexing the outputs of two APV25 chips onto a single optical line driver input.
The communication between the ASICs and the outside world is done via an I^2C bus (Inter-Integrated Circuit, Philips Semiconductors).

3 Module Defect Definitions

During the production process a module can suffer different kinds of damage which eventually must be detected in the tests. In the following a list of the main possible defects is given.

Mechanical Defects and Handling Damages. All kinds of defects due to accidents or mistakes in the production fall into this category; the possible defects include touched or broken wire bonds, scratches, notches or stains on the silicon surface or edges, missing components on the bias kapton circuit, broken pitch adapters, glue excess preventing assembling or bonding or installation.

Noisy Channels. Those readout channels which exhibit noise which is consistently higher than the expected average for a standard module, in such a way that they can greatly deteriorate the capability of reconstructing a particle signal on that channel, are considered noisy.

Dead Channels. Readout channels which do not respond properly to calibration signals and have a very low noise are considered dead.

Open Channels. The *opens* are readout channels that are not connected to the corresponding sensor strip due to a missing wire bond between the pitch adapter and the sensor (or the APV25), or an interrupted PA track.

Short Circuit Channels. The *shorts* are two or more neighbouring readout channels that are shorted together due to defects such as scratches on the silicon sensor surface, unwanted metal contact between strips, problematic wire-bonds or PA tracks.

Metal Strip Breaks. These are interruptions in the metallization of the strips, which can cause a module efficiency loss.

ASIC and Electrical Defects. The ASICs on the modules can have electrical or soldering defects which usually show as problems in communication, addressing or readout. Modules having an abnormal LV current consumption are included in this category.

APV25 Defects. These are defects which are strictly related to the APV25 behaviour. Possible defects are pipeline cell non-uniformities, non-working inverter channels, gain variations outside specifications.

Silicon Crystal Bias Current Defects. There is a class of defects which may usually cause a large increase in the current when applying the voltage bias. These are defects on the sensor, such as scratches, notches and contaminations due to mishandling. Possible defects include also unwanted connections between the sensor backside (or sensor cut lines) and low reference voltage parts of the module.

Pinholes. Pinholes (PH in the following) are anomalous connections between the p+ implant and the metal strip above the implant; as a consequence the coupling between the implant strip and the APV25 input is no longer purely capacitive, but it has a DC component. Pinholes may be due to imperfections in the dielectric layers separating the implant from the aluminium strip, or due to damages made by handling or bonding tools.

4 Measurement Definitions

The basic measurements and inspections used in the IT centres to determine if a module could be considered as suitable for installation in the CMS Tracker are described in the following list.

Optical inspection. This is a detailed visual inspection by eye and followed by a deeper inspection with a microscope to spot damages to the silicon sensor, to the hybrid or to the wire bonds.

Pedestal measurement. The pedestal is defined as the average value of each APV25 channel output when no signal is applied at its input. This measurement gives the baseline profile of each APV25, which does not depend on the connection of the pre-amplifiers to the silicon crystal.

Noise measurement. The noise is calculated as the root mean square deviation of each APV25 channel with respect to its pedestal value after subtraction of the baseline shift common to the whole APV25; the standard deviation of this common shift is known as Common Mode Noise. Measurements are done in all of the APV25 operation modes described in Section 2. This test is used for the identification of dead channels (which have a noise close to zero), or intrinsically noisy APV25 channels (roughly a factor 1.5 higher than the expected average). It also provides some useful indication for identifying opens and shorts.

Pulse Shape measurement. The APV25 has internal calibration circuitry to inject charge in each pre-amplifier channel. The full pulse shape can be reconstructed varying the injection time with respect to the main 25 ns chip clock. The pulse shape measurement can be analysed to extract the peak time and the pulse height of the APV25 output, which are then used, together with the noise measurement, to identify opens, shorts and PHs.

Silicon bias current versus applied voltage (I-V). This measurement checks the I-V characteristics of the module and verifies that a predefined current limit of 10μA is not reached up to the maximum test voltage. Since the I-V is measured also on a large majority of the bare silicon sensors, both at the production firm and in CMS sensor quality test centres, comparisons before and after module manufacturing are made in order to identify possible newly introduced defects.

APV25 Pipeline test. Noise and calibration response are evaluated for all of the APV25 pipeline cells, in order to verify their uniformity and stability.

LED test. This test produces large charge signals on the implant strips, on the far end with respect to the readout hybrid, by means of infra-red light; it was intended to find possible breaks in the metal strips.

Specific Pinhole Test. To find PHs, infra-red diodes were used. Those diodes generate a variable current in the silicon crystal as a function of light intensity. Pinhole identification is very important because of the intrinsic risk of letting undetected pinholes in the final detector. Pinholes may, in the worst case, prevent the normal functioning of an entire APV25. A simplified circuit of a readout strip in the standard case and in the case where a pinhole is present is reported in Fig. 4. The total maximum photo-current generated by the infra-red diodes over the detector is around 500μA ($\mathrm{I_{leak}}$); this current gives a voltage difference of approximately 1V on the p+ implant of each strip with respect to ground, because of the voltage drop over the strip bias resistor, whose average value is about 1.5 MΩ [8]. In case there is an ohmic contact between the aluminium strip and the underlying p+ implant, the same voltage level on the p+, neglecting the voltage drop on $\mathrm{R_{PH}}$, will be present on the metal and then directly at the input of the APV25 pre-amplifier, which will consequently

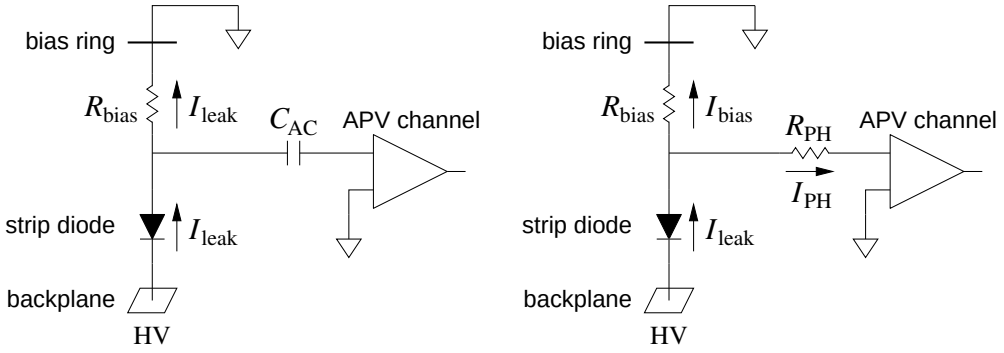

Figure 4: Simplified schematics of a normally working strip (left) and a strip with a pinhole (right). C_{AC} is the strip decoupling capacitor.

be at a different working point than the design one. In this situation the APV25 will exhibit an abnormal behaviour which can be detected by means of internal calibration measurements taken at different photo-generated currents, allowing PH detection.

The overall defect tagging is achieved by combining the results of the above described tests; the combination criteria also depend on the tests that are available at each production stage.

5 The Hardware Equipment for Module Test: ARC and Long Term Set-ups

The hardware used for the tests described in this paper was standardized following the CMS Module Test Working Group prescriptions, in order to have the same facilities in all testing centres. The ARC system [13] (developed by III. Physikalisches Institut B, RWTH Aachen University) was adopted for all the single module short term tests, extending from simple hybrid testing up to fully microbonded module testing. To perform Long Term tests, where in this case "Long" means order of one to three days, in different environmental conditions, all the test centres were equipped with CMS prototype electronics for module control and readout, and a remotely controlled active climatic chamber which could house up to ten modules. Both the ARC and LT equipment have the possibility to fully investigate the characteristics of the module under test, in terms of driving and readout of the module electronics; they even have the capability of monitoring and controlling bias and supply voltages and currents of the modules. Both ARC and LT can also perform, if needed, more specialized and deeper tests, other than the ones described in Section 4. Regardless of the hardware used, the results were always stored in ROOT files. Subsequent analyses evaluated in detail all the measurement results and extracted relevant parameters to be uploaded to the Tracker Construction DB.
Having at each testing location the same hardware provided the TIB/TID community with a common base to achieve the necessary coherence and uniformity of results. Moreover in order to reach this goal the appropriate procedures were established and pursued in each laboratory, and a reference module was tested in all TIB centres to verify the compatibility of results obtained on the same specimen. The quality control procedures described in this paper comply with the quality assurance required by the complexity of the CMS experiment, and have been shown to be efficient for tracing back any defect or damage found during module production.

5.1 Tests with the ARC Setup

5.1.1 ARC Hardware

The standard ARC system is based on a main ARC board, connected to an interface card sitting in the ISA (Industry Standard Architecture) bus of a personal computer running Windows (version 2000 or XP), and linked to the module under test via a front-end board. The graphical user interface, data acquisition and analysis tools are based on LabVIEW [14]; the software application is called ARCS (APV25 Readout Controller Software) [13]. The system needs to be powered externally with $\pm$ 5V. In addition the ARC includes as complements a dedicated HV power supply and an infra-red LED pulser. The HV card (named DEPP [15]) has two independent HV channels, capable of providing a bias voltage between 0 and 600V with a current up to 1mA; it is used to reverse bias the silicon detector. The LED pulser can set the diode current between 0 and 100mA; output pulse duration and

repetition rate can be chosen according to experimental needs. The system includes diodes and optical fibres. Both DEPP and LED pulser are fully controlled by the ARCS. During testing the module was placed in an aluminium box, and flushed with clean dry air to keep the relative humidity below 30% to protect the module from external humidity, which can cause high leakage currents. The box provided also shielding from light and from possible electromagnetic noise induced by external sources. A picture of the full ARC setup is shown in Fig. 5, including DEPP and LED cards and a bar code reader used to read in the module identification number. The black metal cover (clamshell) visible on the right of the picture was kept close during tests.

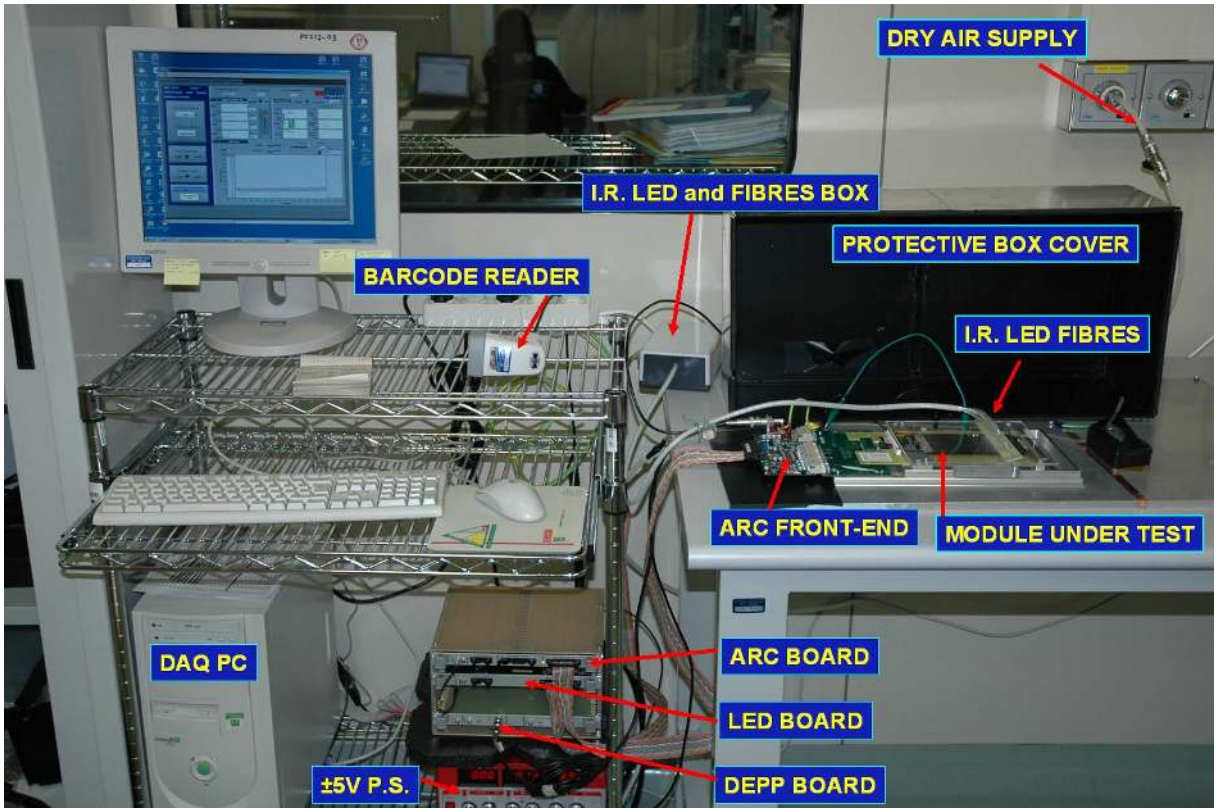

Figure 5: Overview of the complete ARC setup in a clean room with a module ready to be tested.

5.1.2 Single Tests

The ARC system could perform many different tests, such as those reported in Section 4, which could be selected individually according to the specific global action required. For each single measurement the operator could define all of the operational parameters and the threshold levels for module qualification, according to the type of object under test. All the parameters which the ARC software used for discriminating bad channels were loaded at initialization with a single setting file specific for each module type. The flexibility of testing with the ARC system allowed us to define the optimal set of measurements to be done at each production stage as described in Section 6.

5.1.3 Fast Test

The most basic test that the ARC could do was the "Fast Test". It included nine functionality checks aiming to spot major anomalies which would directly cause the rejection of the module without continuing the following time consuming production steps. The Fast Test verified minimal module (or hybrid) functionalities, including I^2C communication, ASICs response, LV levels, power consumption, APV25 internal calibration response, pedestal and noise. Once the module was on the test bench, the time needed to run a Fast Test was less than one minute.

5.1.4 Full Test

The "Full Test" was a thorough and extended test of all module functionalities. During the Full Test the ARC sequentially measured pedestals, noise, Common Mode noise and calibration pulse shape in all four APV25 operation modes. The test sequence included also a pinhole test in Peak Inverter Off and a LED test in Peak Inverter On. A pipeline test was performed for reference. An I-V curve up to 450V was also recorded, with a selectable voltage ramp-up speed. Environmental variables such as temperature (on the silicon sensor, on the hybrid, on the ARC front-end card) and humidity were recorded. At the end of the Full Test the ARCS powered off both HV and LV on the module to allow for a safe disconnection. The time required to run a Full Test was about 20 minutes.

5.2 Tests with the Long Term Setup

The LT system was conceived and optimized to perform the measurements required to identify those defects which can arise during the initial period of operation of the module. Weaknesses, mechanical or electrical ones, and malfunctions, are more likely to appear in the early working period of each module, especially under thermal stress conditions. All the tests have been performed at nominal working voltage settings; we choose to avoid electrical stresses by overvoltage. For the silicon bias the voltage of 450V was never exceeded, although all the sensors are rated for at least 600V bias. The basic tests were the same as for the ARC system, except for the tests involving the LED system which was not implemented in the LT setup. The LT system had several additional features which allowed for efficient testing of up to ten modules in one go: the possibility to repeat the tests as many times as needed in a user selectable way, the recording of all local environmental and electrical variables at programmable time intervals, and the automatic control of the thermal cycles.

5.2.1 LT Hardware

In the LT system the modules were housed inside the climatic chamber on their standard aluminium support plates as shown in Fig. 2. The chamber shown in Fig. 6, the so-called "Vienna box" (since it was devised and produced by the HEPHY Vienna group [16]), is a thermally insulated box made of plastic and aluminium; it houses two 300W liquid-cooled Peltier elements on top and bottom sides, which are able, under computer control, to cool or heat the interior in the range between -30°C and +70°C. An additional external chiller was used to bring the Peltier cells coolant down to 5°C for better cooling efficiency. All the signal and power lines of the modules inside the

Figure 6: The Vienna cooling box filled with six modules ready for a LT test.

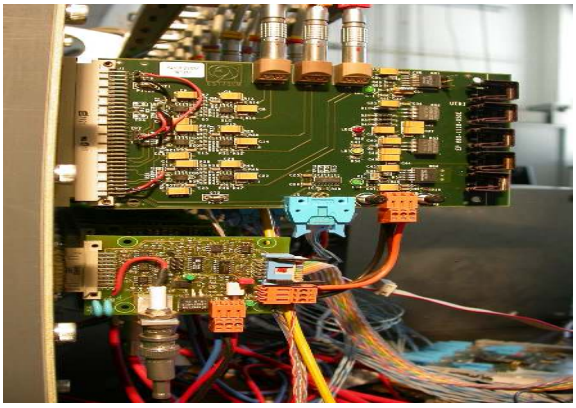

Figure 7: VUTRI (top) and PAACB (bottom) cards inserted in the cooling box backplane.

Vienna box are routed through the box backplane and are connected outside to the data acquisition system via a set of custom boards (VUTRI, or Very Ultimate TRigger Interface-card, Fig. 7) providing LV regulation and buffering of the output analogue signals. A second set of custom boards (PAACB, or Power Adapter And Control Board, Fig. 7) provided the connection for HV and LV power lines; it also measured LV currents and temperatures on the modules (reading the same thermistors cited in Section 2). The communication between the control PC and the PAACBs was done via the I^2C protocol.
The DAQ (Data AcQuisition) was based on an industrial PC housing all the input/output boards. The basic acquisition cards, prototypes of the final CMS ones, were: the Trigger Sequencer Card (TSC) [17], the Front End

Controller (FEC) [18], and the Front End Driver (FED) [19]. The TSC provided clock and trigger signals for FEC and FEDs, and had I^2C channels available for communication with external devices. The FEC controlled the CCU chip which then managed clock, trigger and I^2C for the modules; up to six modules could be connected to a single CCU card, therefore two CCUs in a token ring communication structure were needed to handle ten modules in the cooling box. The FED is a 40MHz, eight channel, flash Analogue to Digital Converter (ADC) used to convert the analogue data coming from the detector (two multiplexed APV25s per channel). Data lines coming from the detectors and buffered in the VUTRI were routed towards the FED through a 10:1 multiplexer (KMUX, for Karlsruhe Multiplexer) to strongly reduce the number of needed FED ADC channels. Commercially available power supply units provided LV and HV to the modules. A TRHX system [20] (acronym for Temperature Relative Humidity and Communication), connected to the serial port of the DAQ PC, measured temperature and humidity inside the cooling box, on the module support plates and in the surrounding environment. The relative humidity inside the box was kept below 4% at any temperature to avoid water condensation or ice formation, by flushing dry clean air or nitrogen. The TRHX included Digital to Amplitude and Amplitude to Digital converters, and also Digital Input-Output channels, which were used to steer the Peltier cells power supply during thermal cycles. The LT software made use of the data coming from TRHX to control the thermal cycles and handle possible critical conditions. The LT system also had independent interlocks, sensing temperature and humidity inside the box, with user selectable hardware thresholds.

5.2.2 Test "Scenario" and Settings

The required steps and tests for the LT were selected in a command file named "scenario". The scenario contained the instructions to perform each individual test, to change temperatures in the cooling box, to issue I^2C commands, to name and to save data records in ROOT format. The hardware and software parameter configurations needed to run the LT scenario were defined in a set of three xml files. These setting files contained all the information about the hardware components and their connections, the parameters to be uploaded to the modules ASICs, the thresholds for excluding modules from the readout in case of persistent failures, the alarm levels to interrupt the LT procedure, and the working parameters for both DAQ and slow control electronics.
After some trial and optimization work based on the experience of each participating laboratory, all the TIB/TID centres had been using the same scenario and setting files during the same production periods. Scenario files were then coherently modified during module production to perform the LT test in more severe thermal conditions, and also to optimize the test duration.

6 The Test Sequence

Given the complex structure of distributed workload, as outlined in Section 1, it has been necessary to define specific set of tests to be performed at each step of the module production, using the appropriate hardware setup, according to the following list:

- ARC test before module assembly;
- ARC test after module assembly;
- Reception test at bonding centres;
- Full ARC test (or "Deep Test") after bonding;
- Long Term test after bonding.

The details and the sequence of tests adapted to each particular production phase are described in Section 7 and Section 8. The first test in the above list was performed on hybrids at gantry centres, while the rest was performed on modules. All but the LT tests included as first step the ARC fast functionality test.

7 Test at Gantry Centres

The qualification of the module started from its individual components. One of them is the hybrid circuit shipped to the assembly centre already fully functional and assembled with its pitch adapter. For about two hundred modules at production start-up, all the basic tests used to certify the functionality of the hybrid circuit were performed both before and after the actual mechanical assembly of the module. The gantry procedure consisted of the precise

glueing of the silicon sensor and the hybrid circuit onto the carbon fibre support frame [5]. The electrical tests performed before and after the assembly were identical and no change was expected in the performance of the circuit. Any deviation could be a symptom of a potential failure in the assembly procedure. A local database was used to store all the output of the performed tests. No electrical information from these tests was loaded into the Construction Database.
Before the start of the production phase, both Perugia and Bari assembly centres successfully did a cross-calibration process in which the same hybrid was tested carefully with the ARC system.
A detailed protocol was used for each operation in order to ensure uniform procedures and quality; the operations can be summarized in the following three phases:

- Reception and test before assembly:
  - registration of the hybrids in the Tracker Construction Database;
  - visual inspection of each hybrid under a stereo microscope to verify the integrity of cable, connectors, ceramic and pitch adapter;
  - Fast Test for the basic functionalities;
  - Full Test for a more in-depth analysis of the hybrid performances.
- Module assembly.
- Test after assembly:
  - Fast Test and Full Test.
- Shipping:
  - packaging of the module;
  - registration of the module in the Construction DB;
  - shipping to the bonding centre for the next construction phase.

As an example, a typical Common Mode subtracted noise profile is shown in Fig. 8 for a hybrid circuit with 512 channels in Peak Mode Inverter On. Any channel outside the acceptance range would be marked as bad. The hybrid circuit noise acceptance range was between 0.4 and 1.3 ADC counts. Identical criteria were adopted for each measurement during the Fast and Full Tests. In the Assembly Centres, the possible effects of two actions were

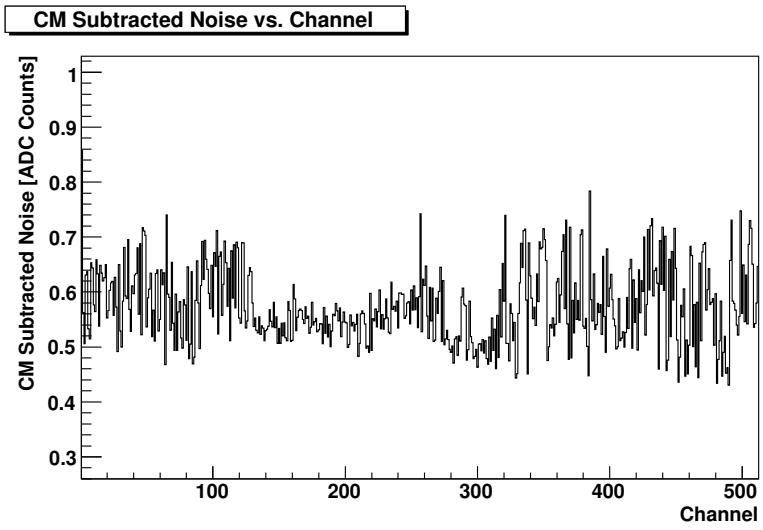

Figure 8: Profile distribution for the Common Mode subtracted noise (Peak Mode Inverter On).

investigated: the transportation from the hybrid production centre and the module assembly itself. All the hybrids were tested beforehand at the hybrid production centre, and the results were sent to the gantry centres along with the hybrid. Any deviation from the results obtained at the hybrid production centre or from the tests performed before the module assembly induced a thorough investigation of any damage produced during the handling of the

hybrid or the module assembly. In such a case, the hybrid or the module was set aside for repair.
After the first 176 assembled modules (82 and 94 produced at the Perugia and Bari assembly centres, respectively) the results (both for Fast and Full Tests) were carefully analysed for possible discrepancies between the tests performed before and after the module assembly. Figures 9 and 10 show the channel-by-channel difference of the Common Mode subtracted noise before and after the module assembly in Deconvolution Mode Inverter On and Peak Mode Inverter On, respectively; both distributions peak at zero with a RMS around 0.1 ADC counts. The

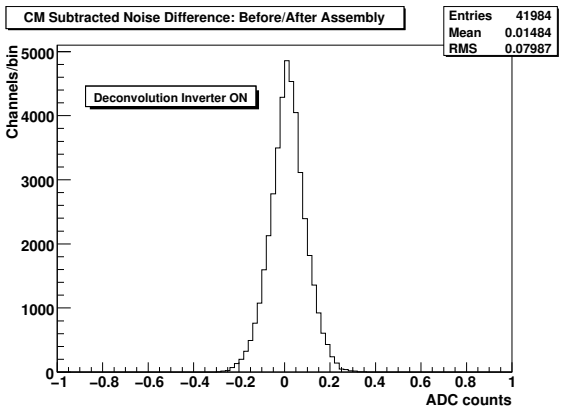

Figure 9: Channel-by-channel Common Mode subtracted noise difference before and after module assembly (Deconvolution Mode Inverter On).

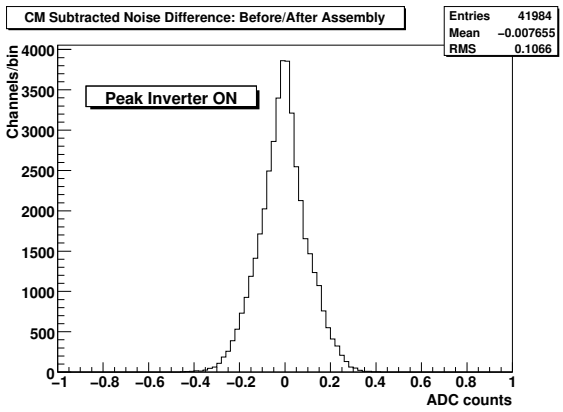

Figure 10: Channel-by-channel Common Mode subtracted noise difference before and after module assembly (Peak Inverter On).

assembly procedure was therefore considered safe and the test following the assembly was done on a sample basis from then on (one module out of each transportation box, which contained nine modules); all the modules were anyway optically inspected.
A total of 3923 accepted modules have been produced in Bari and Perugia assembly centres, providing enough modules for the Inner Tracker. The total number of tested hybrids (before assembly) is reported in Table 1 along with the number of failing ones. More than 50% of the failing hybrids were discarded during the Fast Test (mainly due to APV25 chips not responding, DCU test failures or I^2C problems). The remaining discarded hybrids mainly had mechanical problems such as smashed bonds or damaged pitch adapters.

Table 1: Total number of tested hybrids in Bari and Perugia assembly centres.

	Bari			Perugia		
	Total	Rejected	Yield	Total	Rejected	Yield
Hybrids 4 APV	812	11	98.7%	836	9	98.9%
Hybrids 6 APV	1171	27	97.7%	1183	32	97.3%
Total	1983	38	98.0%	2019	41	98.0%

8 Test at Bonding Centres

The testing of modules at bonding centres was the most detailed and time consuming part of all the test procedures. The procedures foresee that each single module must be inspected and tested both before bonding and, in much greater detail, after all bonding operations have been successfully completed. At the end of this testing phase the module must be ready to be inserted in the Inner Tracker shells and disks or be rejected. We describe in the following all the steps performed at the bonding and test centres to qualify a module for installation.

8.1 Interface Cards

In order to easily connect the module to both ARC and LT setups, two interface adapter cards were designed. The first and smaller one, named “erni-nais” adapter from the connector producer company names, was mounted at the

Figure 11: Erni-nais adapter (on the left of the picture, top and bottom side card views) and VUTRI adapter (on the right of the picture, top side card view).

hybrid assembly factory on the hybrid connector and it was intended to protect the hybrid kapton cable connectors from the stresses due to the multiple insertions occurring during the various testing operations; it was not removed until the final module installation. The second one, named "VUTRI" adapter, connected the erni-nais adapter directly to the ARC or LT inputs via a VME-like connector; both adapters are visible in Fig. 11. The VUTRI was definitely removed after the LT test was completed. The module always remained mounted on a G10 (glass reinforced epoxy laminate) holder during all test and bonding operations.

8.2 Acceptance procedure

Each pre-assembled module, mounted on a transport cradle, arrived at a bonding centre shipped in a plastic box from a gantry assembly centre. Each box contained up to nine modules which were protected against mechanical shocks by a packing foam. After arrival the box and the modules contained therein were registered into the Tracker Construction DB, they were controlled to spot major damages which may have occurred during shipment and then they were stored in a clean room.

8.3 Pre-bonding: Optical Inspection and Rapid Test

The first action was an accurate optical inspection as defined in Section 4. The module was then dismounted from its transport cradle and mounted on a test support plate, which mechanically holds the module (Fig. 12); the VUTRI adapter was permanently installed on the plate. A plexiglass cover was finally screwed onto the plate to provide protection to the module upper side. The cover has a slit to let the diode light reach the sensor. After the optical inspection, the module underwent a first electrical test using the ARC system, called "Rapid Test"; at this stage the

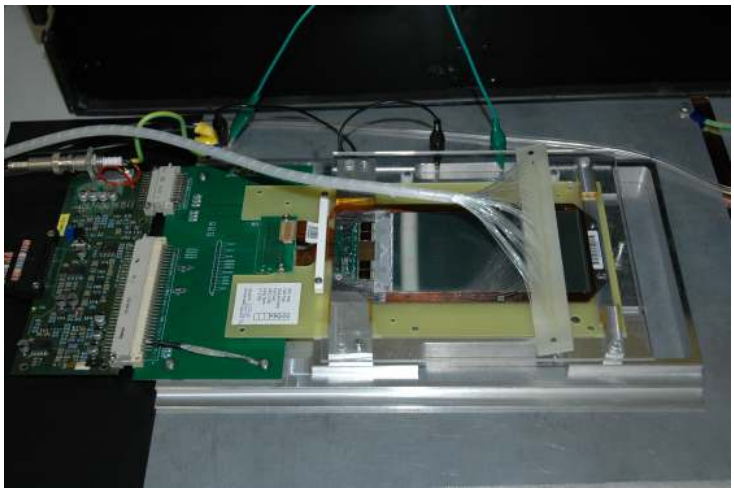

Figure 12: A TIB IB2 module connected to the ARC front-end board. The aluminium test support plate, the G10 module holder and the optical fibres for pinhole test are visible.

sensor had not been connected to the front-end electronics and only the hybrid with the pitch adapter was actually tested. This test consisted of a Fast Test used to spot gross anomalies followed by a more accurate Deep Test which had a duration of less than 10 minutes. The latter consisted of a subset of the Full Test measurements described in Section 5.1.4. In particular pedestal, calibration pulse shape and pipeline runs were taken with the APV25 working in Peak Mode Inverter On. The purpose of these tests was to check the integrity of the pre-assembled module after the shipping and before the sensor microbonding. At this stage the bare APV25 behaviour could be recorded for the last time. Data taken were recorded locally for a possible future use, but they were not uploaded to the Tracker Construction DB. The decision if a module passes this test was taken automatically by the ARC software, using the thresholds suitable for a non-bonded module. These thresholds were given in the same setting file adopted for hybrids test. If the module passed the rapid test it was handed on to the microbonding station.

8.4 Test after bonding

8.4.1 The Special Test Procedures for Start-up Production

Before starting bonding operations [21] the module was dismounted from its aluminium support plate and mounted on the bonding jig. In the early phase of mass production (first 30 modules per centre on average) we decided to first bond the silicon detector bias lines (bias ring and backside) and then perform again a rapid test followed by an I-V measurement; afterwards the module went back to the microbonding station where all bonds between the strips and pitch adapter were made. We followed this procedure to identify possible effects coming directly from bonding action of the HV lines, which required bonds on top and bottom faces of the module and some risky manipulation. The procedure aimed also to spot possible sensor damages occurring during assembly operation, when no measurement with HV bias applied to the sensor could be done.
The results from about 180 modules did not show any increase in the number of defects with respect to the not-yet-bonded module, or worsening of the I-V curve of the module with respect to the bare sensor, thus demonstrating that the upstream operations did not introduce any systematic damages to the sensors or to the electronics. For the rest of the module production this intermediate rapid test was then skipped.
The first $\sim$100 produced modules underwent a passive thermocycle after full bonding; the modules were cooled down to -10°C. Up to six modules were mounted in a suitable air-tight box which was flushed with nitrogen or dry air to keep the relative humidity below 2% and then the box was inserted into a commercial fridge. The modules were not readout during this "passive" cooling, but the full ARC test was repeated once the modules were back at room temperature. No effect was seen on the module performance, and since all the modules had to undergo the full long term test with severe thermal cycles, this passive cold test was eliminated from the final production procedures.

8.4.2 The Standard Test Procedures with ARC

The fully bonded module, once again on its support plate, was connected to the ARC system as shown in Fig. 12 and placed in the clamshell. The grounding connections of the setup were optimized to reach a Common Mode noise RMS below 0.4 ADC counts when the APV25s operate in Peak Mode Inverter Off. Such low noise level is important to correctly identify the different defects. An example of a Common Mode Noise distribution matching this requirement is shown in Fig. 13. First a "Fast Test" was performed. After the "Fast Test" an I-V curve was recorded in the range of 0-450 V using 10 V steps with a six seconds interval between two consecutive points: if the module did not reach the maximum voltage with a current lower than 10 μA, it was investigated. If the reason for the high bias current could be found and the defect eliminated, the module was fully tested again; in all other cases the module was rejected. Whenever possible the I-V curve of the module was compared with the one measured on the bare sensor (corrected for temperature differences) stored in the Tracker Construction Database. In case of a module bias current (at 450V) increase greater than a factor five with respect to the bare sensor value, even if the maximum current value did not exceed the 10 μA threshold, the module was considered problematic and set aside for further investigations. An example of the I-V curves for a TIB module and its corresponding bare sensor is reported in Figure 14. When the I-V measurement completed the module was biased at 400 V again and all the remaining tests of Section 4 were sequentially done. All the information coming from the Full Test was kept on disk at each testing centre for reference. The ARC Full Test lasted about 30 minutes; at the end it issued the number of bad channels together with summary plots and quantities relevant for module qualification. When necessary and possible the module was sent back to the microbonding machine operator for repair and then it was re-tested. The analysis programs described in Section 8.6 can be run on the produced ROOT files, for a detailed classification of defects and to store a reduced set of information characterizing the module in the Tracker Construction Database.

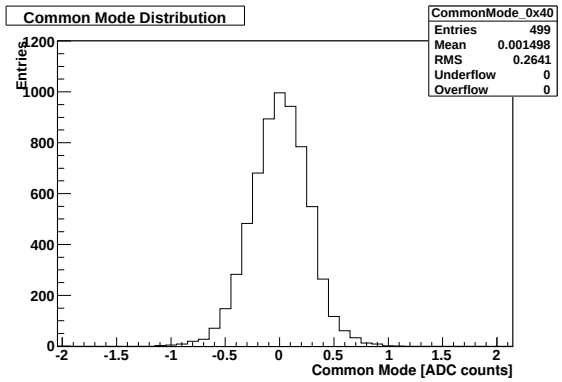

Figure 13: Typical distribution of Common Mode for an APV25 (Peak Mode Inverter Off) matching the test requirement (RMS less than 0.4 ADC counts).

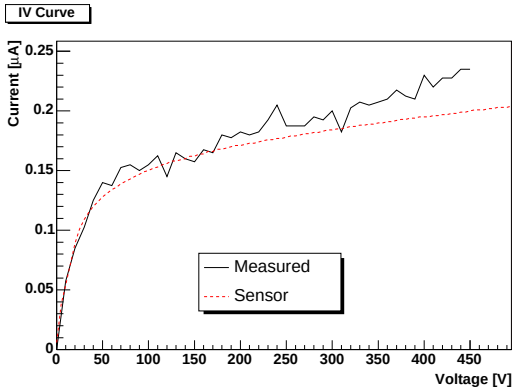

Figure 14: The I-V curve of an assembled and bonded TIB module ("Measured", full line) compared with the one measured during sensor quality tests ("Sensor", dashed line). The sensor curve is smoother than the module test curve due to the smaller voltage step between measurements.

8.4.3 The Procedures for Long Term Test

The underlying concept of the Long Term Test was to keep modules in operation as long as compatible with the production schedule, while varying the temperature inside the box volume. The delay between module bonding and LT test was kept short (a few days at most) in order to minimize impact on the number of already built modules in case of discovery of systematic problems traceable back to the production chain. The LT test duration was chosen to be about three days, consistent with other silicon microstrip detectors such as CDF [22] and D0 [23], for the first few months of module production in 2004; this duration allowed nine thermal cycles between +20°C and -20°C to be performed. These ones were the target temperatures of the sensed spots in the cold box itself. The temperatures on the sensor and on the hybrid were somewhat higher, as will be seen in Fig. 22 (Section 9), due to the temperature gradient between the module and the cold plates of the Vienna box. All the modules in the cooling box were always clocked and powered (both LV and HV); trigger signals were sent during pedestal and calibration runs. Pedestal and calibration runs were taken at each target temperature point, and pedestal runs also in between, when the temperature was rapidly varying. When the box reached -20°C a command (named Hard Reset) to switch off the analogue section of the APV25 was issued; without analogue power the hybrid temperature reached a value between -5°C and -10°C. The system was kept in this condition for one or two hours, then the modules were re-initialized and pedestal and calibration runs in all four APV25 working modes were taken. This particular procedure aimed to verify that ASICs control was never lost even at temperatures around -10°C and that the re-initialization was still effective in this condition. A full I-V scan was performed nine times at -20°C and three times at +20°C, measuring the current on the High Voltage power supply channels, with a resolution sufficient to spot major problems (e.g. currents above a few μA). Every set of measurements was stored in the same ROOT file, for a total of 19 records for this type of scenario. The first record and the last record at +20°C, named respectively MODULLTFIRST and MODULLTLAST, and the last record at -20°C, MODULLTCOLD, were used for uploading results into the Tracker Construction DB. No systematic failure was observed during the LT test, with the above procedures, of a few hundred modules in all TIB/TID centres. In particular no new pinholes appeared during LT tests. For these reasons the scenario file gradually evolved by intermediate steps towards shorter time durations. This process, in the second half of year the 2005, ended up in a one-day long scenario, including the same tests and main records for the DB as described above, but with only two cooling cycles to -20°C. In this way all the TIB/TID modules have been LT tested for at least one day.

8.5 The Selection Criteria for Production Modules

After an initial learning phase, during which about two hundred modules of different types were tested, we came to a set of cuts to be applied to Inner Tracker modules to identify bad channels, based on the measurements of noise, pulse shape with APV25 internal calibration, pinhole test and I-V curve; the test results were combined to arrive at the final module grading. In Table 2 the selection cut values on the noise measured with ARC are reported, along

with the corresponding defect classification, to be used for the module qualification after bonding. The cuts were optimized according to module type and APV25 operation mode. Ring 2 modules needed different cut values, having a shorter strip length. The channels at the edge of each APV25, were not included in the bad channels list,

Table 2: Selection cut values on noise (N) and defect identification with ARC.

Module Type	TIB, Ring 1, Ring 3	Ring 2	
	Noise limits in ADC counts		Defect
PEAK Mode	$N \leq 0.65$	$N \leq 0.65$	PH
	$0.65 < N < 0.95$	$0.65 < N < 0.85$	OPEN
	$N > 1.45$	$N > 1.35$	NOISY
DEC Mode	$N \leq 1.00$	$N \leq 1.00$	PH
	$1.00 < N < 1.30$	$1.00 < N < 1.25$	OPEN
	$N > 2.10$	$N > 1.90$	NOISY

if they were only flagged noisy. As a matter of fact the APV25 edge channels may suffer from non-perfect module grounding and during both LT and ARC tests they were slightly noisier than the average of the module, as can be seen from Figs. 17 and 18 in Section 8.6. In order to strongly reduce this effect and to get a better grounding, a copper-beryllium lid connecting the hybrid ground to the carbon fibre frame, visible in Fig. 3, was added to each module before installation on substructures. Noise measurements performed on the full Tracker structures showed an almost complete suppression of the noise increase at APV25 edges, and this suppression confirms the soundness of excluding noisy edge strips from the bad channel list. To identify pinholes we relied mainly on the difference between the maximum and minimum amplitude of the calibration signal during the ARC pinhole test, which is an indication of a change in the APV25 response, induced by the photo-generated silicon current when a pinhole is present. The defect was classified as pinhole if the above mentioned difference in amplitude was higher than 40 ADC counts. The noise figure was considered as a confirmation only.
Eventually a channel was classified as bad according to the pulse shape measurement, if its calibration amplitude was less than 85% of the APV25 chip average value, or if the peaking time deviated more than 5ns from the average peaking time of the entire module.
The selection cuts reported in Table 3 were applied to the LV currents, since an anomalous power consumption has been shown to be an indication of possible subtle problems in the APV25, and actually the current measurement was already part of APV25 wafer testing [24]. A few modules with dead APV25 channels, probably caused by electrostatic discharges during the handling or the bonding process, showed an increase of the order of 100mA from the 2.5V rails. The cuts in Table 3 were applied already at ARC Fast Test level, and all the modules falling outside those limits were classified as bad, although no evidence was found of degraded performance even during the LT test.

Table 3: Range of allowed values for Low Voltage currents (Ampere).

4APV Modules	6APV modules
$0.19 \leq$ Current $1.25\text{V} \leq 0.26$	$0.29 \leq$ Current $1.25\text{V} \leq 0.37$
$0.45 \leq$ Current $2.50\text{V} \leq 0.57$	$0.65 \leq$ Current $2.50\text{V} \leq 0.78$

The same overall selection philosophy was applied to the module LT tests, using slightly different cut values because of the different hardware components, as described in Section 5.2.1. The LT software had the possibility of excluding from the DAQ those modules which did not respond properly to the I^2C commands, or which had too many bad channels, or LV and HV currents outside limits. The exclusion from the DAQ, after a preselected number of trials, was necessary to avoid slowing down the whole LT test of the full batch of modules. In these cases the excluded modules where carefully inspected, re-tested with ARC and then, in case of no evident failure, again LT tested. In most cases the reason for exclusion was traced back to a non-optimal contact between the support plate connector and the cooling box backplane feedthroughs, which meant the module itself had no defect. However, if those modules were again excluded during a new LT test in a different cooling box slot, they were classified as bad.
Examples of the results from the ARC tests, performed at bonding centres, are presented here; these examples can help understanding the eventual module defects and give an idea of significant cuts to identify them.
The ARC Fast Test output screen, reported in Fig. 15, shows all the results of measurements performed during a complete Fast Test; in this particular case the module under test did not pass the Fast Test because it had too

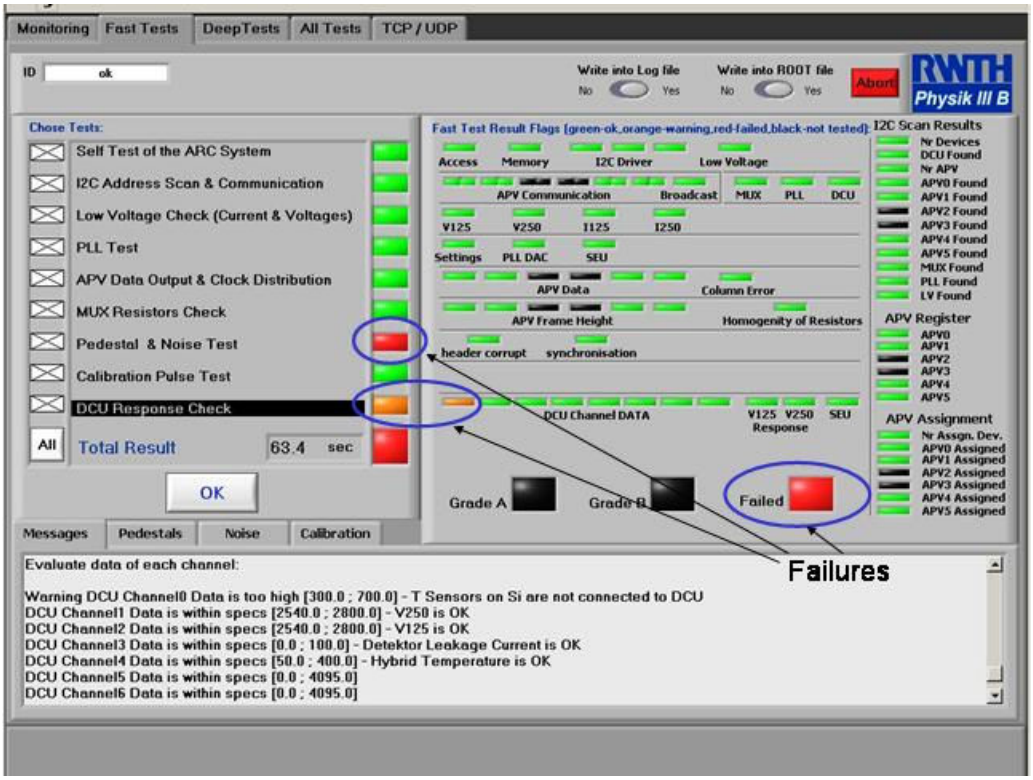

Figure 15: ARC Fast Test Summary display.

many bad strips (not shown in the picture). The ARC found also that the thermistor readout through the DCU gave a result outside limits (DCU Response Check, highlighted). This defect can be cross-checked looking at the readings of the sensor temperature via the DCU in the upper right mini-window of Fig. 16: the plot line stays flat at 4095 ADC counts, which is the maximum of the full scale DCU converter, and this behaviour is an indication of a missing or not connected thermistor. In Fig. 16 there is a screen-shot of the main monitoring view of ARC, with the four APV25 output frames superimposed and directly visible on the screen in scope mode; the APV25 output frame consists of a 3-bit digital header, 8-bit pipeline address, one error bit, 128 samples of analogue data and one synchronization pulse. Behaviour of currents, low voltages and temperatures are also shown in mini-windows of Fig. 16. In Fig. 17 the noise profile of a six-APV module is shown, which has two channels flagged as noisy and one flagged as open. The cut values for noisy and open channels are superimposed on the profile. The noise profile of a module with a pinhole defective strip is shown in Fig. 18: the noise of strip number 388, tagged as a pinhole, is more than 30% lower than the noise of an open strip such as the one visible in Fig. 17. In Fig. 19 the calibration pulse amplitude is shown for the same defective strip (number 388) as in Fig. 18: as expected (Section 5.1.2), a large variation of the amplitude as a function of the infra-red light intensity is clearly visible. For reference, in Fig. 20 the standard calibration amplitude is plotted for the strip next to the pinhole during the same test.
A screen-shot of the LT monitor display is reported in Fig. 21; the display shows the temperature and the relative humidity (RH) variations of different elements of the setup during a nine thermal cycles test. The RH inside the box (lower part of the bottom graph) is rapidly falling to zero, within the RH sensor sensitivity limits. An example of the module temperatures, as measured and stored in a ROOT file by the LT setup, is shown in Fig. 22.

8.6 Module Qualification and Grading

All the Inner Tracker module test results were analysed with a custom software tool, named xFLAG, expressly written to this purpose. xFLAG analyzed the ROOT files written by ARC and LT and combined pieces of information from different tests; it assigned a “defect code” to each defective channel found, and it provided the final grading of the module. It produced an xml file in a format ready to be uploaded to the CMS Tracker Construction DB. Grading was done separately for ARC and LT results; in case of disagreement the worst grading was kept for final validation. The detailed meaning of the module final grading keys stored in the DB is reported in Table 4 for reference. For each defective strip found, xFLAG assigned a defect code to the strip and both the code and the strip number were written into the DB. The association between defect type and its code is reported in Table 7.

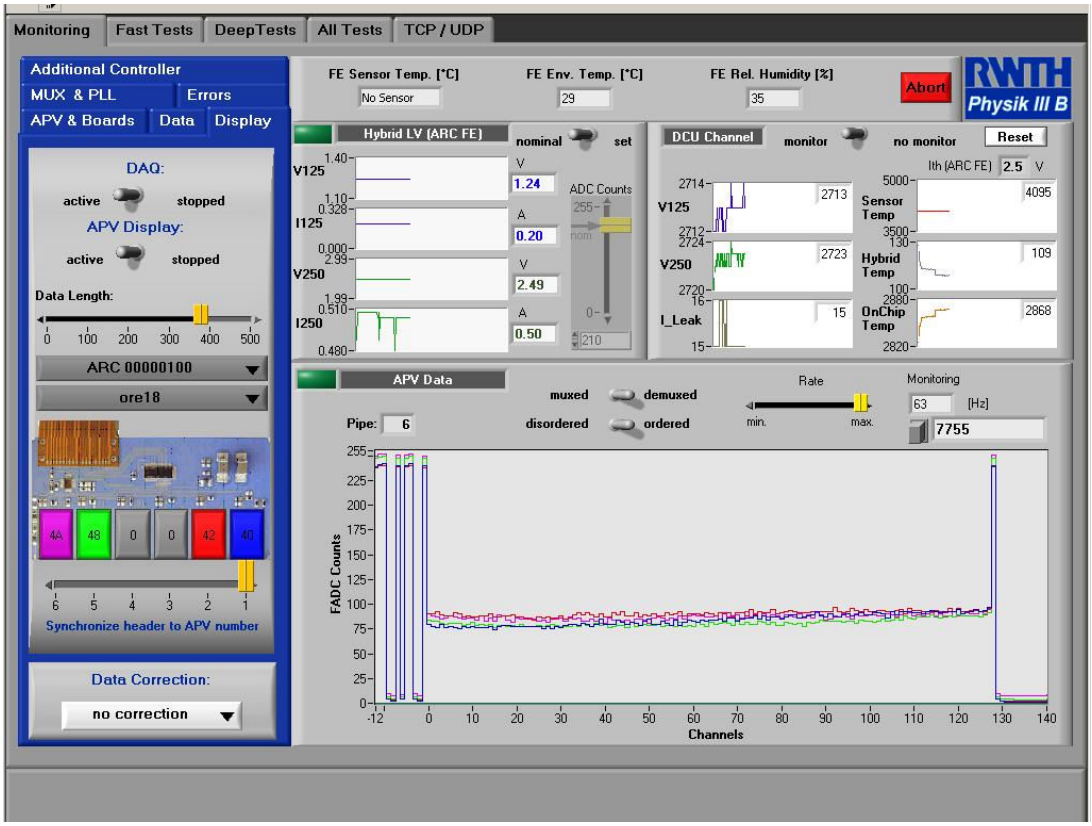

Figure 16: ARC Monitoring screen-shot.

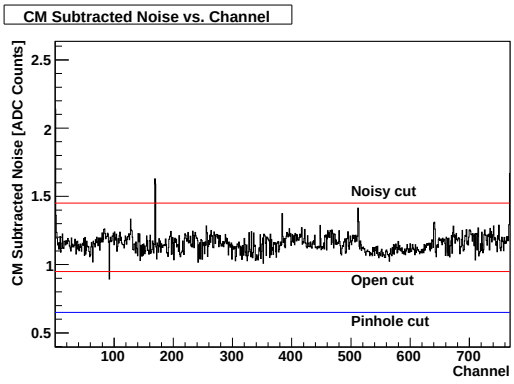

Figure 17: Noise profile of a module with open and noisy strips.

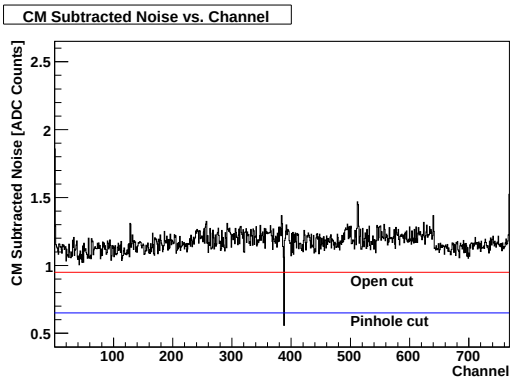

Figure 18: Noise profile of a module containing a pinhole.

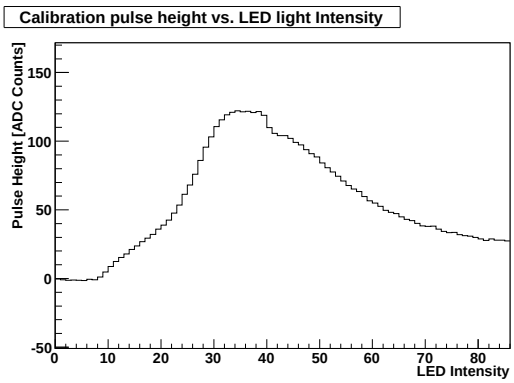

Figure 19: Calibration amplitude on a strip (number 388 of the module shown in Fig. 18) with a pinhole. LED intensity in arbitrary units.

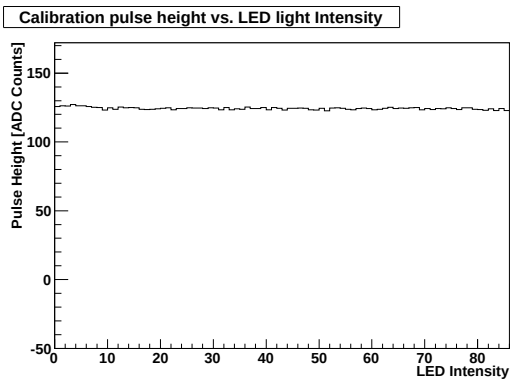

Figure 20: Calibration amplitude on a normally working strip (number 389) next to the pinhole strip. LED intensity in arbitrary units.

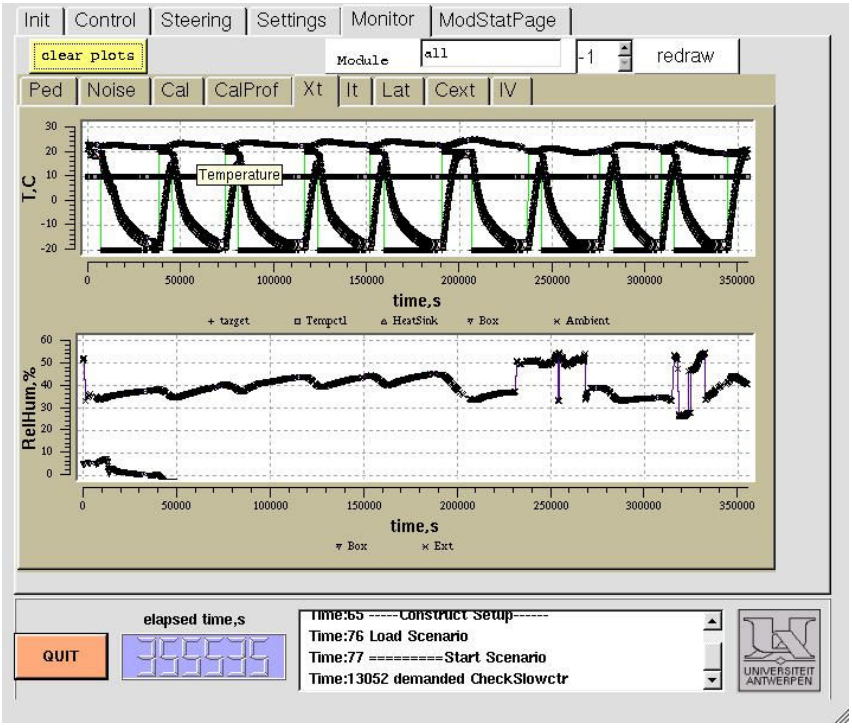

Figure 21: Screen-shot of the LT monitoring program. Upper graph: temperatures of box cold plate, external environment, and set points. Lower graph: relative humidity outside and inside the cooling box.

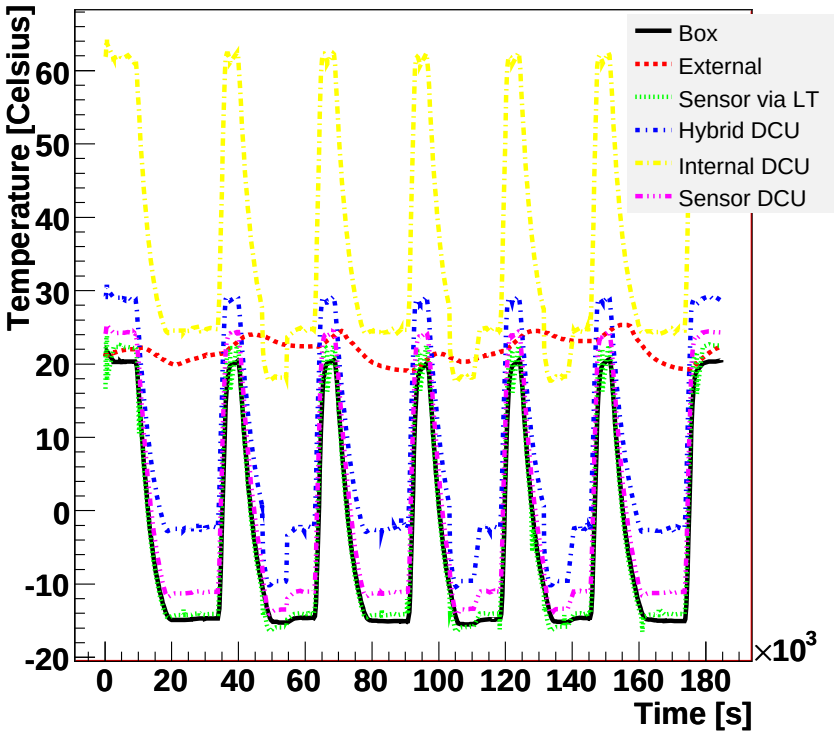

Figure 22: Temperatures recorded by the LT setup for a six-APV module. Temperatures are measured at the points indicated in the legend. The effect of the hard reset (Section 8.4.3) is visible in the second, fourth and fifth cold cycle, producing a 7-8 °C decrease of the Hybrid temperature.

Table 4: Summary of module grading keys. Classes A to BF correspond to accepted modules; class C corresponds to rejected modules.

Grade	DB Key Value	Condition Matched
Accepted Modules		
A	0	$N_{bad} \leq 1\%$
AF	2	$N_{bad} \leq 1\%$ AND $I_{bias} > 5 \times I_{sens}$
B	4	$1\% < N_{bad} \leq 2\%$
BF	8	$1\% < N_{bad} \leq 2\%$ AND $I_{bias} > 5 \times I_{sens}$
Discarded Modules		
C	-1	$N_{bad} > 2\%$
C	-2	$I_{bias} > 10\mu A$
C	-4	$N_{bad} > 2\%$ AND $I_{bias} > 10\mu A$
C	-8	No readout possible
C	-16	Mechanical damage
C	-32	Dismounted from substructures

9 Global Results

A summary of all the produced modules, including bad ones, is reported in Table 5. The analysis and the plots presented in this paper are based on modules whose records are in the status "reference" in the Tracker Construction DB. In this case the word "reference" means that the module has completed all the tests and it has been assigned its final grading. The Inner Tracker consists of 2724 TIB modules and 816 TID modules and we qualified for installation 3814 modules. The overall fraction of rejected modules during final production, for all possible reasons, extracted from the DB is equal to 3.1%.

Table 5: Summary of Inner Tracker module production from Construction Database.

	Accepted	Rejected	Yield
TIB	2915	101	96.7%
TID	899	23	97.4%
Total	3814	124	96.9%

It is worth mentioning that there have been modules production batches which, after detailed tests and thorough discussion of results within the CMS Tracker community, have not been considered acceptable for installation. The weak points were in the hybrid circuit which had three different problems. The first one (discovered in September 2003) was a weakness of the traces in the Kapton cable housing the connector; the second one (December 2003) was related to ASIC's bonds, made by the hybrid assembling company, below specifications; the third one (April 2004) showed up in certain electrical connections between different layers (called vias) which could break under thermal or mechanical stresses. About 4800 hybrids, a fraction of them being already assembled into modules, were affected in the whole Tracker. As a very conservative reliability measure, those hybrids and modules were not qualified because of the potentially dangerous defects found; they are not included in the tables and plots presented in this paper.

A very basic indicator of the module quality is the silicon bias current, since most of the mistakes or mishandling done during the module production process can cause a bias current increase. The bias current in the following plots is the one measured by the ARC ammeter. In Fig. 23 the bias current for all the ARC validated modules is plotted, showing a remarkably low average value around 300 nA. In Fig. 24 the distribution of the bias currents including the bad modules (all defects) is reported for comparison; the range is extended to the maximum allowed bias current of 10μA. As can be seen in the plot, a very small number of modules have bias current above 1μA.

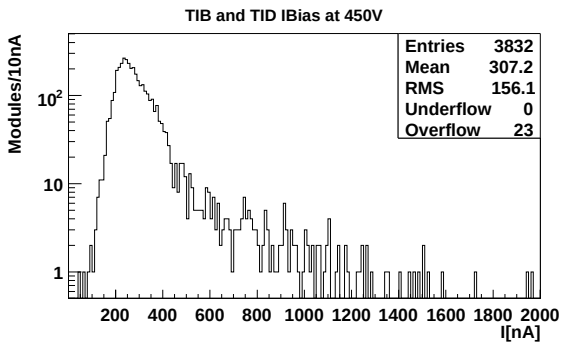

Figure 23: Silicon bias current for all validated TIB and TID modules from ARC deep test.

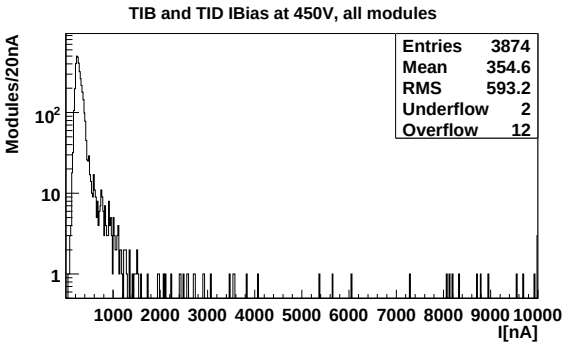

Figure 24: Silicon bias current up to ten μA for all TIB and TID modules from ARC deep test.

The low voltage currents as measured by ARC, for all tested modules including bad ones, are reported in Fig. 25 and Fig. 26. The distributions are rather narrow, taking into account the systematic errors due to the measurements done in different test centres; the current consumption can be influenced by the setting of the APV25 output level, which cannot be fixed once for all as most of the other parameters. Moreover, when the APV25 does not receive triggers for some tens of seconds, its power consumption starts to decrease and the current value measured depends on the time elapsed since last trigger was sent. The two families of four- and six-APV modules are well separated. The arrows in each of the plots indicate the cut values for four (left pair) and six (right pair) APV modules. These

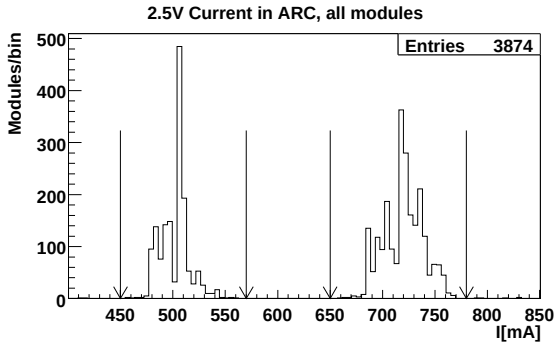

Figure 25: Low Voltage 2.5V currents for all modules from ARC.

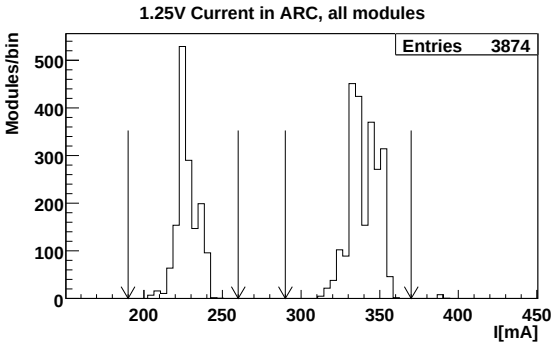

Figure 26: Low Voltage 1.25V currents for all modules from ARC.

distributions can greatly help in estimating the modules power consumption and its spread in the full Tracker.
The calibration pulse amplitude in ARC for all validated modules is reported in Figures 27 to 30. While most of the calibration distributions are single peaked, there is a double peak structure in the data from TIB four-APV modules; the lower calibration peak could possibly be due to subsets of APVs with a somewhat smaller test pulse charge injection. This effect has been confirmed in the LT results, and it is present also in deconvolution mode. The average value of the maximum of the pulse amplitude distribution is equal to 82.9 ± 1.4 ADC counts. The RMS of the amplitude ranges from 9% for TIB four-APV modules to less than 5% for TID four-APV modules.

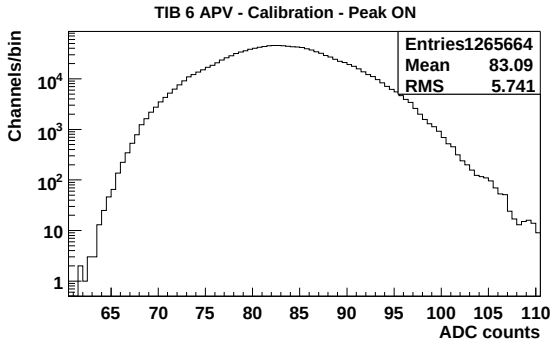

Figure 27: Calibration amplitude distribution for six-APV TIB modules from ARC.

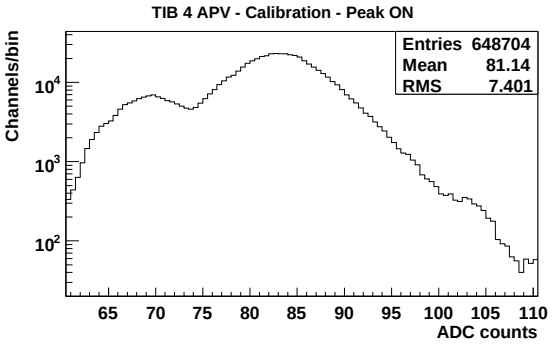

Figure 28: Calibration amplitude distribution for four-APV TIB modules from ARC.

In Figs. 31 to 34 the strip noise cumulative distributions in peak and deconvolution mode for the production modules validated with ARC are shown. The arrows in the plots represent the cut values between which the strips are considered healthy. The peak at small noise values, between 0.5 and 1 ADC counts, is due to the strips which are left not bonded; usually these strips either had some bondability problem, or had a pinhole, or were shorted with nearby strips. In the last two cases the procedures of the MTWG required that, after having identified the defect, the strips were unbonded and then the module tested again, the net final result being an increase in the number of non-bonded strips. The summary of channels classified as bad is reported in Table 6. It is important to remark

Table 6: Summary of channels classified as bad after ARC deep test.

	TIB	TID	Total
Number of Modules	2933	899	3832
Total Number of Channels	1923584	625152	2548736
Number of Bad Channels	1672	492	2164
Fraction of Bad Channels	$8.7 \cdot 10^{-4}$	$7.9 \cdot 10^{-4}$	$8.5 \cdot 10^{-4}$

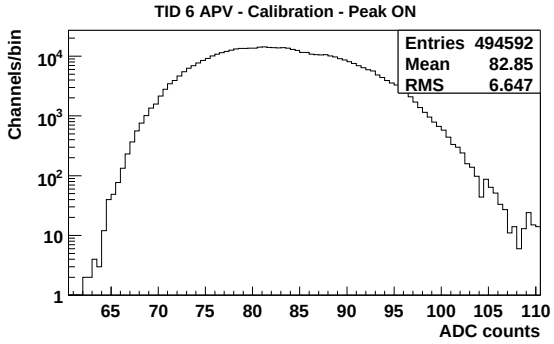

Figure 29: Calibration amplitude distribution for six-APV TID modules from ARC.

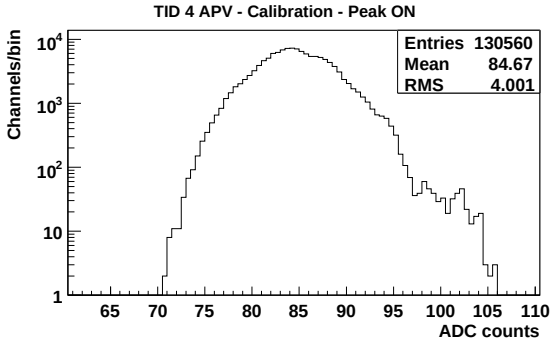

Figure 30: Calibration amplitude distribution for four-APV TID modules from ARC.

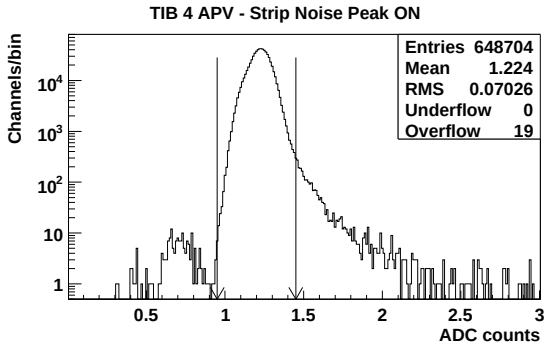

Figure 31: Strip noise from ARC, four-APVs TIB modules operated in Peak Mode Inverter On.

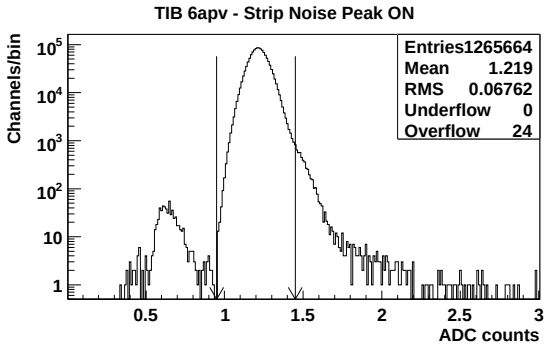

Figure 32: Strip noise from ARC, six-APVs TIB modules, operated in Peak Mode Inverter On.

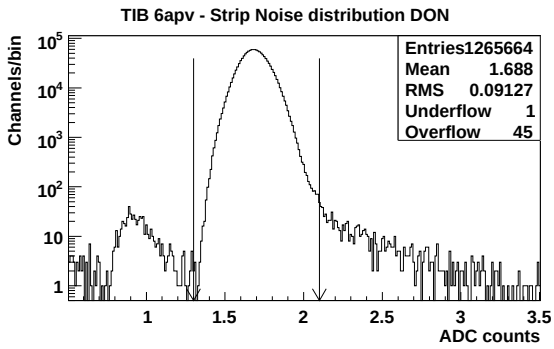

Figure 33: Strip noise from ARC, six-APVs TIB modules operated in Deconvolution Mode Inverter ON.

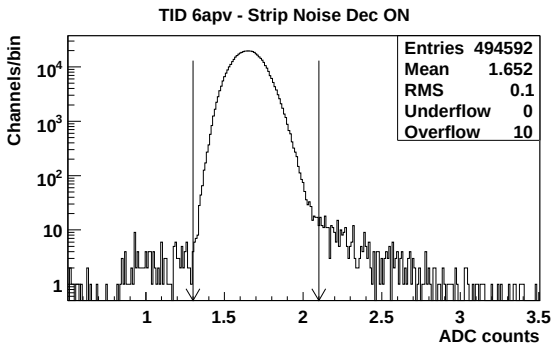

Figure 34: Strip noise from ARC, six-APVs TID modules operated in Deconvolution Mode Inverter ON.

that a large fraction of those channels, namely the ones noisier than the average, can still be used in the detector, with a lower, but still quite acceptable, signal-to-noise ratio with respect to normal channels. The average noise value found in module tests is actually consistent with a signal-to-noise ratio obtained with minimum ionizing particles greater than 25 when operating in peak mode.
The number of bad channels per defect type is shown in Table 7 where in principle no more PH should appear after having unbonded all the corresponding strips following test results. The distributions of the number of bad channels per module in TIB and TID are shown in Fig. 35 and Fig. 36, respectively.

Table 7: Number of bad channels in TIB and TID classified according to defect type. The associated defect code is also indicated.

Defect Type	Defect Code	TIB Channels	TID Channels
PA-Sensor Open Circuit	2	148	165
Likely PA-Sensor Open Circuit	4	630	25
Strip Open Circuit	32	23	9
Noisy Strip	64	719	264
Short Circuit Strip	128	26	8
Likely Pinhole	256	5	1
Pinhole	512	1	1
Multiple Sources Defect	1024	49	7
Dead Channel	2048	43	7
Dead Inverter Channel	4096	28	5

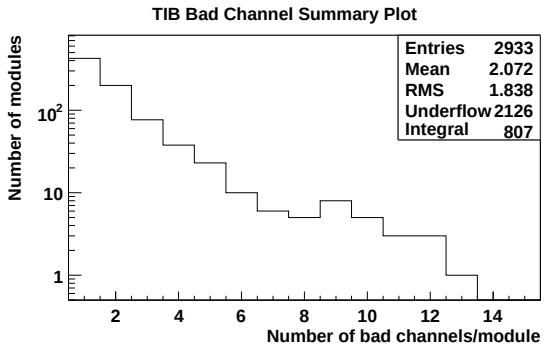

Figure 35: Bad channels distribution in TIB for qualified modules; APV25 edge strips not included. Zero defect modules are indicated by the Underflow figure.

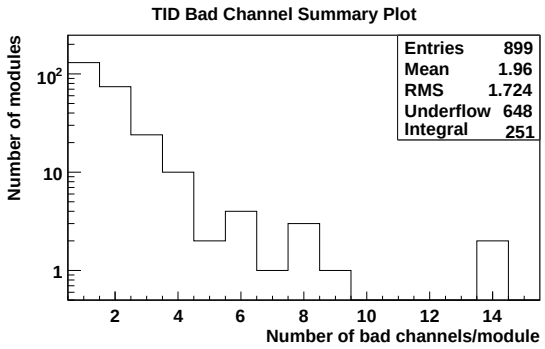

Figure 36: Bad channels distribution in TID for qualified modules; APV25 edge strips not included. Zero defect modules are indicated by the Underflow figure.

10 Conclusions

The Module Test procedures for the Tracker Inner Barrel and Disks have been illustrated, following their evolution from the beginning of module production up to the full mass production. This report accounted for tests at both assembly and bonding centres. Results and examples from each testing step have been shown. The production of more than 3900 silicon microstrip modules, not including the pre-production series, has been a remarkable success. The quality of the modules, as it can be derived from the analysis of the data stored in the Tracker Construction Database, is excellent: less than 1 per mille of the readout channels presently installed in the CMS Tracker has been classified as noisy or not working. The global number of modules which had to be rejected in all test phases up to the installation on Tracker substructures was around 3%. The module test effort, from the initial test definition and development activities down to the last long term tests, involved more than 50 people in seven different centres of the INFN, spanning the years from 2000 to 2005.

References

[1] CMS Collaboration, *"The CMS experiment at the CERN LHC"*, 2008 JINST 3 S08004.

[2] CMS Collaboration, *"CMS: The Tracker Project Technical Design Report"*, CERN/LHCC 98-06, CMS TDR 5, 15 April 1998; CMS Collaboration, *"Addendum to the CMS Tracker TDR"*, CERN/LHCC 2000-016, CMS TDR 5 Addendum 1, 21 February 2000.

[3] R. Brun and F. Rademakers, *"ROOT An Object-Oriented Data Analysis Framework"*, Proceedings AIHENP'96 Workshop, Lausanne, Sep. 1996, Nucl. Instrum. and Meth. A 389 (1997) 81-86.

[4] *"CMS Tracker Database"*, http://cmsdoc.cern.ch/∼cmstrkdb.

[5] P. Cariola et al., *"Assembly of the Inner Tracker Silicon Microstrip Modules"*, CMS NOTE-2008/004.

[6] M. Axer et al., *"The Qualification of Silicon Microstrip Detector Modules for the CMS Inner Tracking Detector*, CMS NOTE-2006/141.

[7] T. Bergauer et al., *"Petal Integration for the CMS Tracker End Caps",* CMS NOTE-2008/028.
W. Beaumont, Universiteit Antwerpen 2005, *"Longterm CMS Si module test",*
http://www.hep.ua.ac.be/cms/testing/software/ltmod/ltmodintro.html

[8] L. Borrello et al., *"Sensor Design for the CMS Silicon Strip Tracker"*, CMS NOTE-2003/020.

[9] M. French et al., *"Design and Results from the APV25, a Deep Sub-micron CMOS Front-End Chip for the CMS Tracker"*, Nucl. Instr. and Meth. A 466 (2001) 359.

[10] S. Gadomski et al., *"The deconvolution method of fast pulse shaping at hadron colliders"*, Nucl. Instrum. and Meth. A 320 (1992) 217.

[11] G. Magazzu et al., *"The detector control unit: An ASIC for the monitoring of the CMS silicon tracker"*, IEEE Trans. Nucl. Sci. **51** (2004) 1333.

[12] P. Placidi et al., *"A 40-MHz clock and trigger recovery circuit for the CMS tracker fabricated in a 0.25μm CMOS technology and using a self calibration technique"*, prepared for 5th Workshop on Electronics for the LHC Experiments (LEB 99), Snowmass, Colorado, 20-24 Sep. 1999.

[13] M. Axer et al., *"Testing of FE Hybrids and Si detector modules for the CMS Tracker"* Nucl. Instrum. and Meth. A 485 (2002) 73.

[14] National Instruments, LabVIEWProfessional Development System for Windows, Linux, Version 6.0, 2000.

[15] F. Beißel, *"DEPP Manual"*
www.physik.rwth-aachen.de/fileadmin/user_upload/www_physik/Institute/Inst_3B/Forschung/CMS/Detektorentwicklung/ARC/DEPP_2.pdf

[16] M. Pernicka et al., Vienna Cooling Box,
http://wwwhephy.oeaw.ac.at/u3w/f/friedl/www/coolingbox/coolingbox_overview.pdf

[17] Institut de Physique Nucléaire de Lyon, *"Trigger Sequencer Card User Manual",*
http://lyoinfo.in2p3.fr/cms/cmstraces/tscweb/tsc.html

[18] K. Kloukinas et al., *"A system for timing distribution and control of front end electronics for the CMS Tracker"*, Given at 3rd Workshop on Electronics for LHC Experiments, London, England, 22-26 Sep 1997.

[19] S. A. Baird et al., *"Design of the front end driver card for CMS silicon microstrip Tracker readout"*, prepared for 6th Workshop on Electronic for LHC Experiments, Cracow, Poland, 11-15 Sep 2000.

[20] M. Friedl, *"TRHX Manual"*, http://wwwhephy.oeaw.ac.at/u3w/f/friedl/www/trhx/trhx_manual_v101.pdf

[21] F. Bosi et al., *"Bonding of the Inner Tracker Silicon Microstrip Modules"*, CMS NOTE-2008/024.

[22] A. Affolder et al., *"Construction report of the intermediate silicon layers (ISL) ladders"*, Nucl. Instrum. and Meth. A 461 (2001) 216.

[23] D. Mihalcea, *"The assembly and testing of the D0 silicon detector"*, Nucl. Instrum. and Meth. A 473 (2001) 49.

[24] M. Raymond et al., *"APV25 Production Testing and Quality Assurance"*, Proceedings of the 8th Workshop on Electronics for LHC Experiments, CERN-LHCC-2002-34, 219-223.