The Front End Electronics of the LHCb Straw Tube Tracker[1]

A.Berkien[a], H.Deppe[b], T.du Pree[a], D.van Eijk[a], G.Fanizzi[a], E.Heine[a], F.Jansen[*,a], J.Knopf[b], A.Pellegrino[a], A.Rausch[b], J.Rovekamp[a], R.Rusnyak[b], J.D.Schipper[a], R.Schwemmer[b], E.Simioni[a], T.Sluijk[a], R.Stadler[b], U.Stange[b], B.Storaci[a], H.Terrier[a], P.Thobe[a], P.Timmer[a], N.Tuning[a], U.Trunk[b], U.Uwer[b], D.Wiedner[b], A.Zwart[a]

[a]*Nikhef, Science Park 105, 1098XG Amsterdam, the Netherlands*
[b]*Physikalisches Institut, Philosophenweg 12, 69120 Heidelberg, Germany*

Abstract

The LHCb experiment is a single-arm spectrometer, designed to study *B*-hadron decays at the Large Hadron Collider (LHC). It is crucial to accurately and efficiently track the charged decay products with the Outer Tracker straw tube detector, in the high-density particle environment of the LHC. The Outer Tracker Front End electronics provide the precise (0.5 ns) drift-time measurement, at an average occupancy of 5% and at a 1 MHz trigger rate. The tracking procedure requires high-efficiency, while at the same time putting stringent limits on the noise level. The mass production and installation of 450 fully operational Front End boxes is completed. Quality checks have been performed at several stages, at the level of individual boards and at the global level with dedicated test systems mimicking the real detector and capable of simulating all the readout functionalities. An excellent overall threshold uniformity is achieved with low noise levels.

Key words: Front End electronics, Tracking detectors, Gas detectors, Straw tubes
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1. Introduction

The LHCb experiment [1] has been tailored for the study of *B*-hadron physics. The Outer Tracker (OT) [1] is a straw tube tracker detector for the LHCb tracking system. The basic OT detector element is a module, consisting of 2 staggered layers of 64 straw tubes of 5 mm diameter and ~5 m length. During operation the straw tubes are flushed with a Ar(70%)/CO_2(30%) gas mixture, while the anode wire is kept at 1550 V. Each module-end (128 straw tubes) is read out by one Front End (FE) electronics box [2].

The FE electronics measures the drift times of ionization clusters. Hit times are digitized with respect to the LHC bunch crossing clock every 25 ns cycle, and stored in a digital pipeline to await the Level-0 (L0) decision. On a positive L0 decision, the data is transmitted via optical link.

The FE electronics is designed to cope with large occupancies. Its time resolution is required to be better than 1 ns. The fact that hit times may take up to 3 bunch crossing lengths is accounted for. The maximum L0 decision rate is 1.1 MHz. The FE electronics is expected to accumulate an integrated dose of 10 krad over 10 years of running.

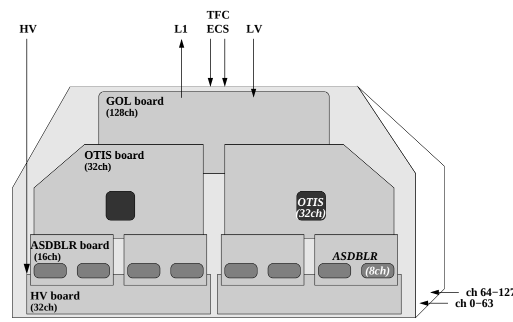

Figure 1: Schematic overview of a Front End box

2. Front End electronics boxes

Figure 1 shows a FE box schematically. It houses 4 different types of circuit boards: High Voltage (HV), pre-amplifier and discriminator (ASDBLR), TDC (OTIS) and serializer (GOL/AUX).

2.1. HV board

The High Voltage board connects to the anode wires of the straw tubes. Pre-resistors of 1 MΩ in front of every channel decouple the anodes from each other and avoid large currents in case of shorts in the straw tubes. The high voltage on the anode wires is decoupled from the small hit charges caused by passing particles by a 330 pF capacitor. The capacitors are embedded in the circuit board to reduce leakage currents.

2.2. ASDBLR

The ASDBLR board amplifies the signals received from the HV board and discriminates them against threshold. The board

*Corresponding author
Email address: fabianj@nikhef.nl (F.Jansen)

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has 2 ASDBLR ASIC [3] (designed for the ATLAS TRT), that were built with the DMILL process and are radiation hard up to a dose of 7 Mrad.

Charge inputs are amplified and passed to a stage of fast signal shaping and baseline restoring (7.5 ns peaking time) to perform cancellation of the slow ion tails that follow the rapid electron avalanche. The signal is discriminated against threshold to obtain a differential output (1 ns rise time).

Care has been taken to minimize noise and cross talk in the design of the ASDBLR board. The process of signal shaping and baseline restoring effectively reduces the dead time to less than 20 ns.

2.3. OTIS

The OTIS time-to-digital converter [4, 5] digitizes the arrival times of the ASDBLR outputs. The OTIS board houses a 0.25 μm CMOS chip, which is radiation hard up to 30 Mrad.

Time digitization is done with the help of delay locked loops (DLL). The DLL's 32 delay elements divide the clock signal into 64 intervals of 390 ps. To determine the arrival time of a hit, the 64 delay stages are latched by the ASDBLR output and encoded into a 6 bit fine time.

The data of 32 channels is written into a 164 stages deep L0 pipeline buffer, which covers the 4 μs trigger latency. Upon a trigger, the corresponding hits are copied into a 16 stages deep derandomizer buffer, which allows for up to 16 consecutive triggers. Here, the fine time receives an additional two bits indicating which of three consecutive bunch crossings a hit is registered in. This allows for an electron drift time up to 75 ns.

A channel mask allows individual channels to be blocked from the data stream.

2.4. GOL/AUX

The GOL/AUX board [6] collects data from four OTIS, serializes it with 8/10 bit encoding and ships it off-detector via a single optical fiber, operating at 1.6 Gb/s. The GOL is a Gigabit Optical Link ASIC, being able to cope with a radiation dose of 1Mrad. Furthermore, the board supplies the low voltage (+2.5 V, ±3.0 V), fast and slow control signals.

3. Front End electronics testing

All FE electronics components have been individually tested and selected before assembly into FE boxes. In particular HV boards were selected with leakage currents below 3 nA (peak below 15 nA) after 48 hrs, at 2000 V high voltage in air and at 70^0. Completed FE boxes have been extensively tested with a dedicated test setup mimicking the real detector and simulating the readout functionalities [7]. The dedicated setup performs tests on 3 basic functionalities.

The threshold characteristics of all channels is measured through a Threshold Scan. The threshold value where the fraction of registered hits is 50% characterizes the sensitivity of a channel. Figure 2 shows the Threshold Scan on FE 409. Boards with at least one channel with a threshold off by ±60 mV (corresponding to about ±0.5 fC) were replaced.

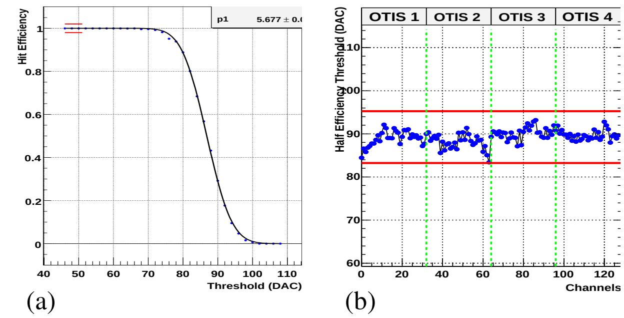

Figure 2: (a) Threshold Scan of channel 1 of FE 409 (5 fC fixed input charge). (b) Threshold uniformity of FE 409. For all 128 channels the threshold values are shown, at which 50% of hits is measured.

A Noise Scan probes the noise levels for different threshold values. Boards with at least one channel with a noise fraction larger than 0.5% at operational threshold of 760 mV (corresponding to about 3.5 fC) were replaced.

Timing behavior of channels is measured with a Linearity Scan. Charges are injected into the FE box at various delays of the LHC clock. The hit time versus delay time gives the linearity of a channel. Boards with non-linear channels were replaced.

4. Conclusion

The OT FE electronics provides precise (<0.5 ns) drift time measurements for the OT detector, with small (<20 ns) dead time. Low noise levels allow low discriminator threshold and maintain the high efficiency of the detector.

The mass production and installation of 450 FE boxes is completed. Quality checks have been performed at several stages, at the level of individual boards and at the global level with a dedicated test system mimicking the real detector and capable of simulating all the readout functionalities.

An excellent overall threshold uniformity is achieved, allowing to run the OT detector at a single amplifier threshold value. During the FE box assembly between 5% and 10% of the boards were replaced, resulting in an OT with fully operational FE boxes.

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