The Front End Electronics of the Scintillator Pad Detector of the LHCb Calorimeter

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Abstract

In this paper the Front End electronics of the Scintillator Pad Detector (SPD) is outlined. The SPD is a sub-system of the Calorimeter of the LHCb experiment designed to discriminate between charged and neutral particles for the first level trigger.

The system design is presented, describing its different functionalities implemented through three different cards and several ASICs. These functionalities are signal processing and digitization, data transmission, interface with control and timing systems of the experiment, low voltage power supply distribution and monitoring. Special emphasis is placed on installation and commissioning subjects such as cabling, grounding, shielding and power distribution.

I. INTRODUCTION

LHCb calorimetry [1] unfolds into four elements: a hadronic calorimeter (HCAL), an electromagnetic calorimeter (ECAL), a Preshower detector (PS) and a Scintillator Pad Detector (SPD). The system provides high energy hadrons, electron and photon candidates for the first level trigger (called L0 trigger) of the experiment.

The PS and the SPD are designed to distinguish electrons from pions and charged particles from neutrals respectively for the L0. PS as well as ECAL and HCAL measure particle energy, whereas SPD is a binary output detector. SPD information is also used to introduce a cut in the L0 on the SPD hit multiplicity for removing the tail of the hit multiplicity distribution (high multiplicity events might clog up CPU nodes), while keeping the same signal efficiency and minimum bias retention.

SPD and PS are two sub-detectors in front of ECAL separated by a 1.4 cm thick layer of lead. They consist in a layer of 6000 plastic scintillator (Bicron BC-408) tiles with a Kurarai Y11 WLS (wavelength shifting) rolled fibre to collect the light emitted by the scintillator when a charged particle goes through it. Charged particles will produce, whereas photons will not, ionization on the scintillator. The light is transmitted through a clear fibre to the SPD readout system. The signal of the scintillator pads, both for PS and SPD, is processed in a Very Front End (VFE) unit. These units are placed on metallic boxes on the top and on the bottom of the respective scintillator walls.

An overview of SPD sub-system and its main connections are shown in Figure 1.

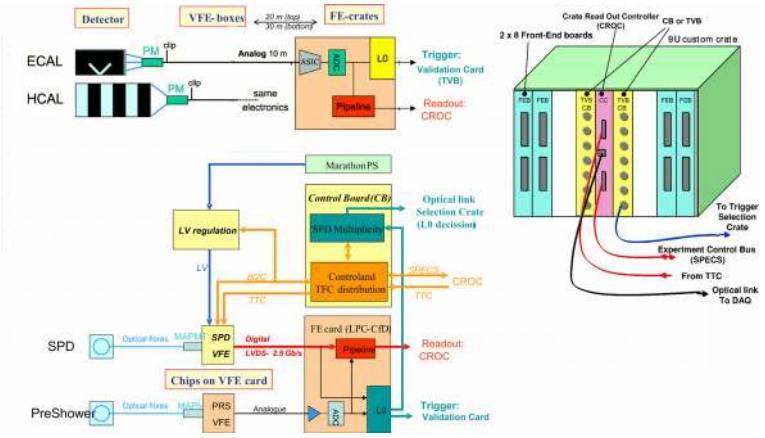

Figure 1. Block diagram of the SPD front-end elements.

The front-end electronics of the LHCb calorimeter [3], except the VFE cards, will be placed in crates at the top of the calorimeters. The total radiation dose expected there is about 6 krads over 10 years thus allowing the use of commercial components, provided that the most critical of them have been tested in a beam. 14 ECAL and 4 HCAL crates receive respectively 6000 and 1500 channels. 8 PS crates receive a total of 6000 channels both from the PS's and the SPD's VFE.

The ECAL/HCAL PM signals are connected directly to the front-end boards (FEBs) through 10 meters of coaxial cables, whereas 20 m to 30 m differential pairs are used to send the output of the PS (analogue) and SPD cards (digital) VFE cards to a common PS/SPD FEB [4]. There are 16 FEBs in the crates, each receiving 32 signals for ECAL/HCAL crates and 64 signals from each detector for PS/SPD crates.

The FEBs have two different data paths: the trigger one and the readout one. The outputs of these boards are connected to the standardized custom backplane, sending signals using LVDS levels to the Calorimeter Readout Controller (CROC) for the readout data path and to the Validation boards for the trigger data path. The CROC also receives the Experiment Control System (ECS) implemented under SPECS protocol [5] and the 40 MHz bunch crossing clock, trigger and synchronous commands from the LHCb Timing and Fast Control system (TFC) [6] and there from distributes them over the whole crate.

The CB is placed in the FE crates; there are two for each of the 8 crates corresponding to the PS/SPD subsystem. The purpose of the CB is twofold:

- To provide to the VFE cards a link to the ECS and TFC system. A phase alignment of the experiment clock [6] is also performed in the CB.
- Each PS/SPD FEB counts the number of SPD hits in the corresponding SPD VFE card. Up to 8 PS/SPD FEBs send this number to 1 CB through the backplane. The CB sums the 8 numbers and sends the result to Selection Crate in barracks.

A water cooled magnetic field and radiation tolerant floating power supply system (MARATON) [7] feeds the crates and the VFE cards. The long distance between FE crates and VFE cards force to use local regulation close to the sensitive electronics. Regulator cards have monitoring capabilities and are also connected to ECS through the CB.

II. VFE Board

As depicted in Figure 2 the VFE board [8] includes a photomultiplier (PMT) to convert the light pulse into charge, the electronics to perform the discrimination between electron and photon signals, a control unit and a LVDS serializer to send the information to the PS/SPD FEB.

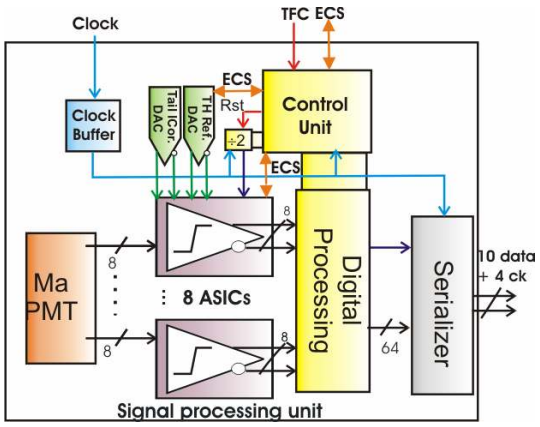

Figure 2. Block diagram of the VFE card

There are two external (no on-chip) DAC with I2C interface to set some analogue references for the signal processing part. The control unit, the digital processing and clock divider to obtain the 20 MHz clock that controls the ASICs operation are implemented through a re-programmable FPGA, the ProAsic Plus Actel APA300. Triple Voting Registers (TVRs) are used to minimize the SEU errors. The digital processing consists on mapping the PMT channel to given serializer channel to match the PS and SPD detector cell (2 different mappings selected by ECS) and to inject arbitrary patterns to test the detector data flow.

The control unit continuously controls SEUs in all VFE registers and signals the errors in a status register. It also allows to power cycle the DACs to recover from SEU hard errors ([2]) in their I2C logic, and provides interface with:

- ECS system between CB and VFE board chips (I2C). According to global LHCb requirements [6], any register can be read back from the ECS.
- TFC system to provide a synchronous reset of the clock divider and trigger for the pattern injection.

A. Signal processing

For economical reasons a multianode (Ma)PMT is chosen as photo detector, being the Hamamatsu R7600-M64 the selected candidate. Acceptance test has been carried out to ensure that the 100 PMTs comply with the specifications [9]. All of the PMT were within specifications for linearity, gain, and uniformity, but not for crosstalk, for which the requirements were not fulfilled for a 10% of the tubes.

The PMT signal is amplified, shaped and discriminated through an 8 channel ASIC [10] (AMS BiCMOS 0.8 µm technology). Figure 3 shows the functional architecture of each channel. The configuration is based on two interleaved processing units per channel to avoid any dead time and to be able to perform the pile-up compensation. The bunch-crossing clock is divided (outside the chip) and then used to multiplex by level the two paths of the channel each 25 ns. To prevent digital crosstalk on sensitive analogue parts, all the blocks are fully differential. Each path uses an independent DAC to be able to compensate the offsets due to process variations between different subchannels.

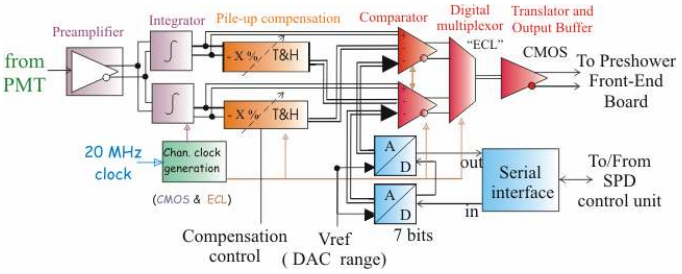

Figure 3. Functional diagram of a discriminator channel.

Techniques were applied to improve the radiation tolerance: place guard rings for MOS transistors to prevent latch up, use NAND gates instead of NOR gates and TVRs to minimise the SEU effects. The chip has been qualified for the LHCb radiation levels [2].

An engineering run was shared with other calorimeter chips to produce about 2000 units, 1300 have been packaged on an EDAQUAD QFP64 package and tested obtaining a yield of the 80 %. Table 1 summarizes the test results of the produced ASICs, for a MaPMT load resistor of 470Ω. A MIP signal will be adjusted through the HV on a 30 to 100 fC range depending on the MaPMT uniformity.

Table 1. ASIC performance

Noise (ENC)	2 fC rms
Gain	1.16 mV/fC
Gain spread	< 5 %
Offset spread	65 mV rms
Correction matching	< 2 %
Linearity Error	< 10 mV (1 %)
Power Consumption	500 mW (3.3 V)

B. Card implementation and performance

As a result of room constraints, the actual design of the VFE board has been split into three different boards as shown in Figure 4.

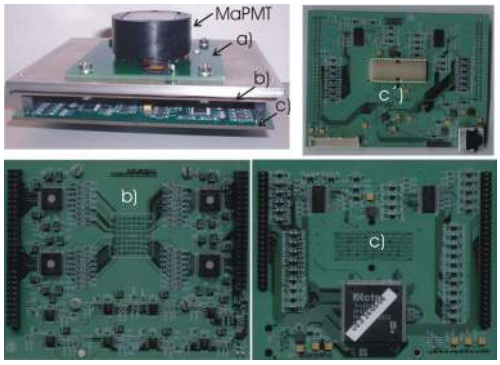

Figure 4. VFE card: a) PMT base board, b) ASIC's board and c) FPGA board (c' is the bottom view of c).

a) *PMT base board*: This board hosts an active base for the photomultiplier.

b) *ASICs board*: This board contains the eight ASICs and its associated circuitry, the part of threshold reference and subtractor reference.

c) *IO/Logic board*: The last board contains the FPGA, the serializers and the connectors.

All components passed radiation tests (see [2] and [11]) in order to obtain the radiation qualification (single event effects and cumulative effects).

A 10% pre-series of a total production of 120 has been produced and tested. The performance of the signal processing in the card is in agreement with ASIC performance summarized in Table 1. The electrical crosstalk is found to be smaller than the 2%. The pedestal short term stability (10 hours operation) is better than 2 mV. A prototype of the card has been tested in SPS facility (X7 area) using a 25 ns clock synchronous with the beam. Although the light yield was low (12 phe/MIP) due to problems with optical connections, a trigger efficiency of 93 % and a fake trigger ratio of 1 % have been measured, setting the threshold at 0.5 MIP. Tail correction and beam phase synchronization were also tested successfully. A total of 9 burn-in cycles of about 8 hours between 0 to 50 ° C have been performed to the pre-series cards and no problematic component has been identified. During the cycles a card was continuously monitored; remaining functional.

C. *Long distance LVDS serialized transmission*

The 64 channels and the 20 MHz clock are sent to the PS/SPD FEBs. The serializing factor in DS90CR215 chip is 7; thus 4 serializers are needed. Since each serializer has 3 data pairs and 1 clock pair, using standard shielded twisted pair (SSTP) LAN cables seems an economic solution.

The skew margin of the serializing chipset is only of 500 ps, and the skew of 30 m long commercial cables is higher than 2 ns, even for category 7 Ethernet cables. However, we observed that the skew between consecutive 30 m cuts of the same pair is very low, usually lower than 500 ps. Taking benefit from the fact that 4 serializers and 4 cables of 4 pairs are needed, we designed a link with a custom board (see Figure 5) implementing a cross-connection scheme to send each pairs corresponding to a given serializer through a different cable but through the same pair.

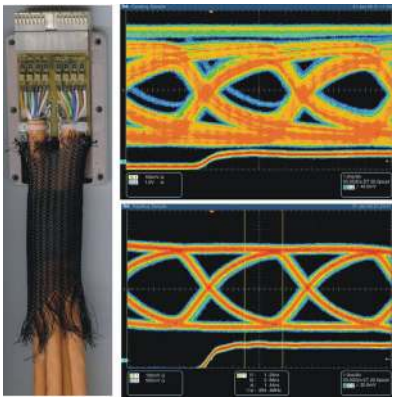

Figure 5. Left: view of the transmitter end of the link. Right: eye diagrams for a category 7 30 m long cable: un-compensated (top) and equalized (bottom) using random patterns.

Since serializer has no pre-emphasis circuit, the card of Figure 5) has a passive (inductor in series with a resistor) pole-zero network to equalize the cable response. An eye opening of 1.44 ns between LVDS thresholds (±100 mV) has been obtained (see Figure 5).

A total number of 120 links have been produced, 64 for the top part (18 m long) and 56 for the bottom part (27 m long). The skew between each data pair and the corresponding clock has been measured. The skew for top cables was smaller than 500 ps. For bottom cables out of 540 data pairs, 2 have a skew between 500 and 700 ps, and 2 a skew of about 800 ps. Only for the pairs with 800 ps skew, errors have been found for some patterns, for other cables BER<10^{-12}.

Furthermore, the frequency clock of the system has been increased up to the limit of the test system which is 60 MHz, without noticing errors for a 30 m long cable. This means that using simple electronics and standard ethernet cables, a copper link can transmit at 480 Mbits/s per pair over 30 m with BER<10^{-14}. The sensitivity of the link to common-mode differences between serializer and deserializer has been also tested, no problem was found in ±0.5 V range.

III. CONTROL BOARD

Figure 6 shows the block diagram of the CB, which is an 8 layers 9U card. As said before we can distinguish between trigger and control functionalities of the CB.

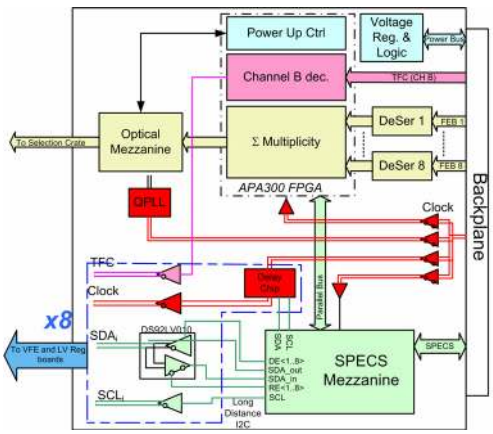

Figure 6. Block diagram of the CB

The trigger functionality consists on receiving and deserializing (DS90CR216) the multiplicity data from up to 8 different PS/SPD FEBs trough LVDS serialized point to point backplane links, adding these numbers and transmitting the information to the barrack through an optical link. The addition is performed through an Actel APA300 FPGA. The optical transmitter is implemented as mezzanine card used in other Calorimeter parts [12]. Data coming from the deserializers can be sampled either at the clock rising or falling edge, this assures a correct sampling provided that the skew between different FEBs is less than half clock period. The multiplicity part has been tested with PS/SPD FEBs placed in all possible slots of the crate.

The control functionality consists on providing ECS and TFC interface for up to 8 VFE elements, either a VFE board or a LV regulation board. The communication between the CB and the VFE element is through SSTP ethernet cables using shielded RJ45 connectors. Therefore, 4 pairs are available: 1 for the 40 MHz clock, 1 for the TFC signal and 2 for the ECS interface.

The SPECS slave is implemented trough a SPECS mezzanine card which is an LHCb standard ECS interface [5]. The SPECS mezzanine provides a standard local I2C bus and a long distance I2C bus. A differential long distance I2C bus over 2 LVDS pairs is the ECS interface for VFE.

The FPGA used for the multiplicity also decodes the channel B lines of the TFC system, where synchronous commands such as resets or calibration pulses are coded. The FPGA serializes a reduced set of commands (see VFE board section) and sends them to the VFE trough a dedicated pair in the control cable.

The remaining pair on the cable transmits the 40 MHz clock to the VFE after being delayed by a programmable clock distribution ASIC [15] to phase align the sampling of the analogue detector signals (integrator's gate is the 20 MHz clock) to the bunch crossings [6]. This chip generates 4 differential outputs and each of them can introduce a maximum delay of 25ns to the clock, with 1 ns steps.

In addition to the trigger multiplicity and channel B decoding, the FPGA perform other tasks. On the one hand, for testing and debugging purposes, the multiplicity data can be spied at the output of the multiplicity part and read through the parallel bus of the optical mezzanine On the other hand, it controls the power start-up sequence of the GOL.

To assure a high quality clock distribution the LVDS clock transmitted through the backplane is point to point buffered with differential drivers placed very close to the input connector. Special care is taken for the clock driving serializers, those for the optical mezzanine and those placed in the VFE card. First problem is addressed filtering clock jitter with a QPLL chip [14] at the input of the optical mezzanine. For the VFE clock a fully balanced differential amplifier (AD8138) is used to drive the twisted pair cable with a pole-zero cancellation network to improve the rise-time of the signal (from 1.2 ns to 600 ps). Table 2 shows jitter measurements for the most important points of the clock network, no degradation is observed neither on the CB itself nor on the VFE board.

Table 2. Jitter results

	Peak to Peak	RMS
Input (test system)	37 ps	4.6 ps
Opt. Mez. Input	33 ps	3.6 ps
VFE (22 m cable)	57 ps	7.9 ps
VFE (29 m cable)	61 ps	9 ps

IV. Grounding, Shielding and Power Distribution

A. Grounding

The calorimeter ground configuration is a heavily interconnected ground network (mesh structure) as recommended in [17]. The electronics of the calorimeter is distributed in many different locations: the front end racks, the PS VFE and the SPD VFE. Although differential signals have been used wherever possible, the input stage of the ASICs is DC coupled to the PMT and it is a single ended signal by definition. Thus, ground parasitic currents should be minimized. This goal should be achieved with a mesh structure with very low impedance from DC to few hundreds of MHz. All cables will be shielded twisted pair.

B. Power distribution

In Figure 7 it is shown the precise power distribution scheme for the SPD. The main power supplies modules are floating and the ground connection is done at the load (regulator card and VFE unit) to avoid returning currents through the ground network.

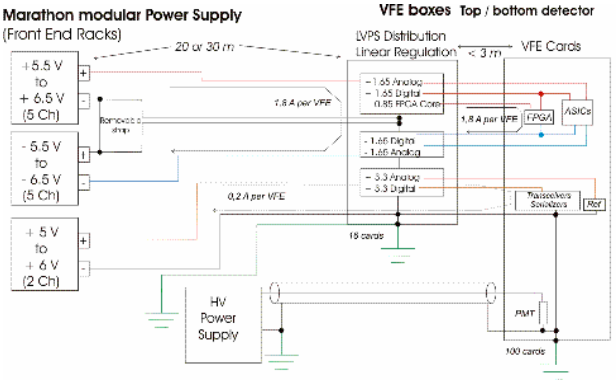

Figure 7. Power supply distribution

Different regulators are used for digital and analogue supply voltages, even if they do have the same value, to minimize conducted interference. It is intended to minimize the current return through the ground network using separated connections for ground and for the current return (neutral conductor) of each power supply. Each power line derived in the Marathon Power supplies and in the regulator card will be protected with a fuse properly tailored to the corresponding operating current to avoid fire or other potential risks in case of short circuit. For the power supply to local regulation connection, shielded twisted pair cables with 4 mm^2 conductor (IEC 60228 class 5 flexible) section will be used. For the local regulation to VFE units short connection, shielded twisted pair cables with 0.5 mm^2 conductors will be

used. Due to the very specific requirement all LV cables are specially manufactured for this application.

C. Electromagnetic Compatibility

The metallic box that houses VFE units and regulator cards should act as a Faraday Cage. The MAPMT/VFE boxes material is iron (5 mm thick).

A potential source of significant inductive noise in the LHCb environment is the coils of the main magnet. The main victims of this interference in SPD VFE could be:

- The MaPMT. The iron box plus a special μ-metal shielding around PMT protect the PMT.
- The inductors used for cable equalization. Special test has been done at Orsay, showing effects smaller than a few % on the inductance up to 400 gauss (worst orientation)

It is not foreseen a specific power filtering for the low voltage connection, the use of local regulation (inside the Faraday cage) is considered to be safe enough. Power filtering is foreseen for the HV in the PMT baseboard.

A VFE box was fully equipped with VFE and LV regulator cards, cabled and tested. No degradation was observed on noise and pedestal stability. The VFE box incorporates a water cooling system that has also been tested with success.

V. LV Regulation Board

LV regulation cards, based on CERN-ST Radiation Hard voltage regulators [16], will be installed in the VFE boxes. The VFE card requires many different supply voltages as reported in section IV.B (Figure 7), making necessary the use of several regulators per card. In order to optimize the usage of the power regulator each regulator card will power up to 7 VFE cards. It results on a complex power distribution system, advising monitoring to be integrated in the same board. This is done using an FPGA which performs periodic analogue readouts of voltages and currents. LV card also performs temperature measurements using onboard probes and probes embedded in VFE cards. A block diagram of the board is shown in Figure 8.

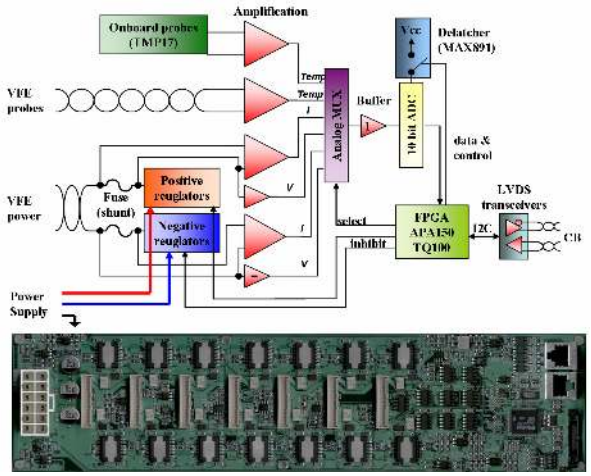

Figure 8. Block diagram and top view of the LV regulation board.

The probability of a SEL is very low but not zero for the serializers (DS90CR215) [11]. In a case of a SEL a real time monitoring system will switch off the regulators. Each power line is also protected with fast fuses. The FPGA also controls the start-up of the logic of VFE board.

A pre-series of the regulation board has been produced and tested. The monitoring instrumentation has been calibrated within a precision better than the 1 % for currents and voltages and of 2º C for temperatures. The same burn-in procedure of the VFE board has been applied. A LV regulation board was continuously monitored through the ECS, remaining operational during the burn-in.

VI. Acknowledgements

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VII. References

[1] S. Amato et alt. "*LHCb Calorimeters Technical Design Report*", CERN/LHCC/2000-0036.

[2] X. Cano et alt. "*Radiation hardness on very front-end for SPD*", Nucl. Inst. and Methods A, 551/2-3 2005.

[3] D. Breton, "*The Front-end Electronics for the LHCb Calorimeters*", Proceedings of the 10th International Conference on Calorimetry in High Energy Physics, 2002.

[4] R. Cornat et alt. "*LHCb Preshower Front-End Electronics Board*", LHCb note in preparation, 2006

[5] D.Breton et al., "*SPECS: Serial Protocol for the Experiment Control system of LHCb* ", LHCb note 2003-004, 2003.

[6] J. Cristiansen, "*Requirements to the L0 front-end electronics*". LHCb note 2001-014, 2001.

[7] M. Plein and A. Köster, "*Power supplies for LHC Experiments for SE and HE application*", Proc. of the 10th Workshop on Electronics for LHC and Future Experiments (LECC), 2004.

[8] S. Luengo et al., "*SPD very front end electronics*", Nucl. Inst. and Methods A, In press, 2006.

[9] E. Aguiló et al., "*Test of multi-anode photomultiplier tubes for the LHCb scintillator pad detector*", Nucl. Instr. and Meth. A 538, 255-264, 2005.

[10] D. Gascón et al. "*A BiCMOS Synchronous Pulse Discriminator for the LHCb Calorimeter System*" Proc. o the 8th LECC Workshop, 2002.

[11] F. Machefert et al. "*LHCb calorimeter front-end electronics radiation dose and single event effects*" LHCb note CALO 2002-021, 2002.

[12] U. Marconi et al. "*The Optical Transmitters for the LHCb Calorimeters*", LHCb note in preparation.

[13] http://proj-gol.web.cern.ch/proj-gol/

[14] http://proj-qpll.web.cern.ch/proj-qpll/

[15] V. Tocut et al., "*A programmable clock distribution chip for LHCb calorimeter*", EDMS 709938, 2006.

[16] http://lhc-voltage-regulator.web.cern.ch

[17] V. Bobillier, J. Christiansen, R. Frei: "*Grounding, Shielding and Power Distribution in LHCb*", , CERN-EDMS 584310, May 2005.