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The high-voltage system for the LHCb RICH hybrid photon detectors

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ABSTRACT

We describe the characterization of the high-voltage (HV) distribution system designed and produced for the pixel hybrid photon detectors of the ring imaging Cherenkov counters of the LHCb experiment. The HV system consists of a series of printed circuit boards with a specific layout designed to prevent any discharge arising from high electric fields. The system has dedicated monitoring and control features to supervise HV set-up during data taking. The full production of the HV system has been now completed and all the boards have been fully characterized and installed in the detector, which is currently being commissioned.

1. Introduction and experimental results

The high-voltage (HV) distribution system for the pixel hybrid photon detectors (HPDs) of the LHCb RICH detectors [1] has been designed, produced, characterized and integrated into the detector. Each of the 484 HPDs, arranged into 32 columns, needs to be biased with three different voltages, −20, −19.7 and −16.4 kV, respectively. Only the −20 kV lines, two for each column of the arrays, are sourced from the control room, a distance of 100 m from the detector. A system composed of printed circuit boards (PCBs), of three different types, manages the input voltages and creates the additional two HV values to bias the HPDs. A schematic diagram that describes all three topologies is given in Fig. 1. The −20 kV voltage line, V_1, feeds each half-column of the array where a PCB with the "splitter" block is found. The splitter block is a customized resistive divider (300 MΩ of total resistance) from which the other two HVs, V_2 and V_3, are generated. The voltages V_1, V_2 and V_3 are then distributed to the other PCBs in the half-column by means of short connecting cables, and to a pair of HPDs via the "HPD bias" block that inserts protective series resistances between the HVs and the HPD input bias lines. Other PCBs of the half-column have only the HPD bias block. The last PCB of the half-column, in addition to the HPD bias block, is equipped with the "monitoring" block. This consists of a set of three resistive dividers to allow the monitoring of the HVs with an attenuation of about 13 kV/V. To prevent any discharges arising from the large electric fields, each PCB is embedded in silicone rubber having a dielectric strength of 17 kV/mm [2].

All PCBs in the system have been characterized. The most important parameter is the leakage current generated, within the silicone rubber, at the soldered nodes which are at HV and drained from the ground. The PCBs have been designed with a tool to study accurately the leakage current. During characterization, the 1 MΩ resistor, R_{sense} of Fig. 1, splits the ground on the PCB into GND1 and GND2. The PCB layout was designed such that the working current through the splitting and monitoring resistors, in the tens of μA range, can flow only through GND1, while the leakage current from the silicone flows from GND2 to GND1 through R_{sense}, across which it generates a measurable voltage. In normal operation, R_{sense} is then short circuited (SC switch) and GND1 and GND2 become a common connection. This allowed a sensitivity in the sub-nA range. Fig. 2 demonstrates the leakage current characterization at a working voltage of −22 kV. A first set of PCBs were subjected to annealing at 60 °C for 3 days. The result is the dashed histogram of Fig. 2, which shows a broad dispersion of the leakage currents. We succeeded in lowering the leakage current value and its spread by increasing the annealing period up to 7 days, and forcing the migration of the residual ions out of the silicone by setting the relative humidity (RH) inside the environmental chamber to 10%. The white histogram of Fig. 2 shows the very good result obtained. The average leakage current is close to 2 nA with a maximum value that never exceeds 5 nA. We estimate a parasitic resistance of the silicone close to 10 TΩ, a value much greater than that of any resistor present on the PCB, to which it can be considered in parallel. As such, a negligible influence on the bias current is expected at any node of the PCB sourcing from it.

Each half-column of the RICH is equipped with a PCB that allows monitoring of the three HVs. The monitoring network consists of three pairs of resistors, 5 GΩ and 392 kΩ, forming potential dividers on each voltage line. The nominal accuracy of each network is ±1%. Our characterization set-up allowed testing two columns at a time, with four monitoring PCBs. In each measurement we had also a reference divider (RD), consisting of 2 GΩ and a 100 kΩ resistors, ±1% tolerance, providing an additional monitoring of the −20 kV

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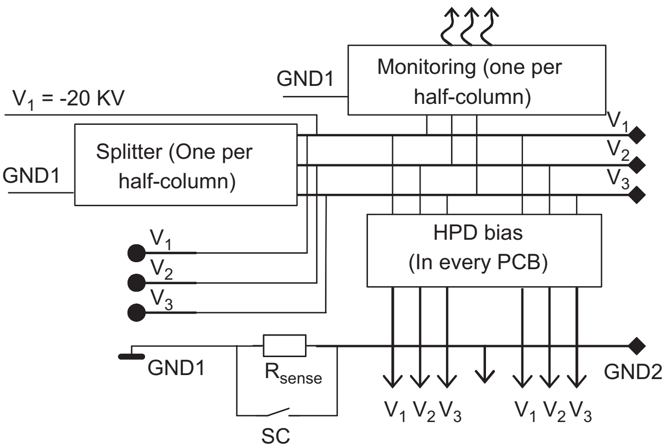

Fig. 1. General schematic of the three topologies of the high-voltage PCB boards.

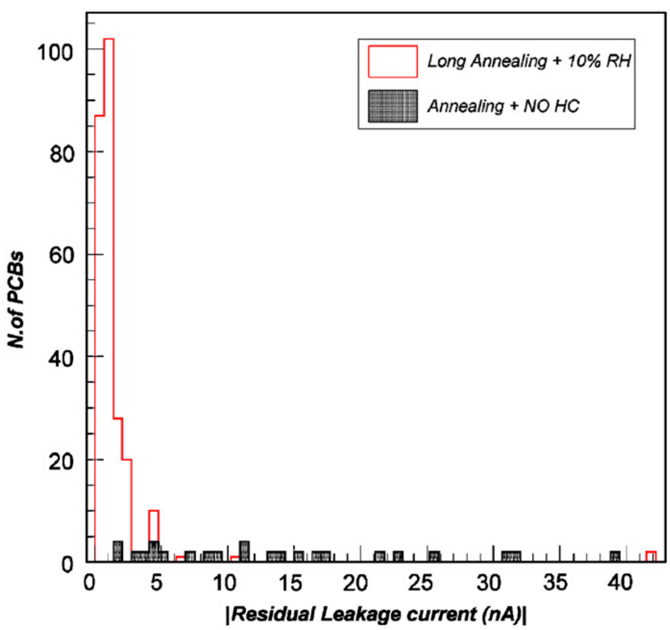

Fig. 2. Distribution of the leakage current from the silicone at -22 kV. The white histogram is measured from the PCBs cured for 7 days at 60 °C—10% RH; the dashed histogram was obtained by a few PCBs cured for 3 days at 60 °C only.

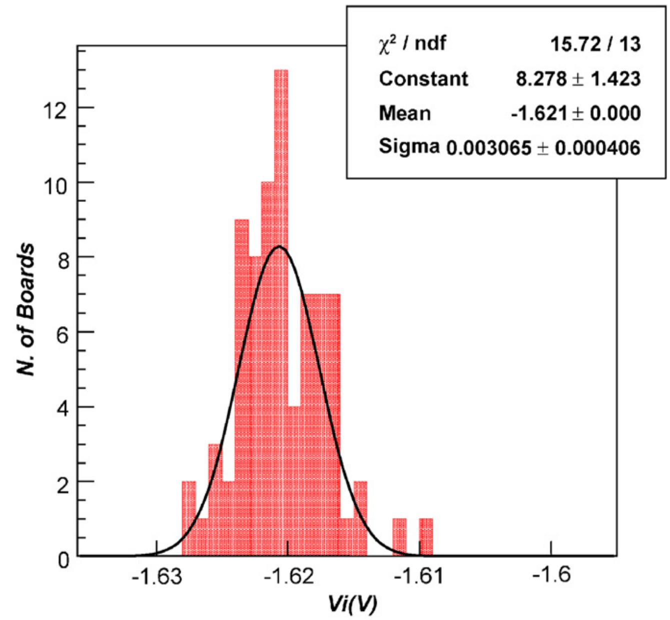

Fig. 3. Statistical distribution of monitoring of V_1 at the divider output.

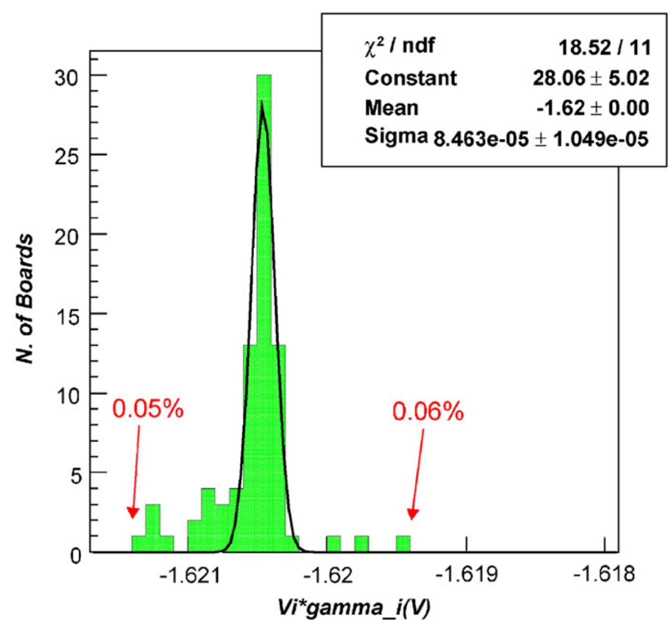

Fig. 4. Statistical distribution of monitoring of V_1, at the divider output, after the calibration method described in the text has been applied.

input line. In addition, the temperature was also recorded during the 2-day test. In Fig. 3, the distribution of monitored PCB outputs is shown, corrected from measurement to measurement with respect to the RD. As can be seen the histogram has an RMS consistent with $\pm 1\%$ tolerance. Similar plots are obtained for the statistical distributions of V_2 and V_3.

Since the voltage V_2, -19.7 kV, is very close to V_1, -20 kV, we tried to obtain a better accuracy, described below.

Although the -20 kV supply, V_1, may vary slightly from test to test, the RD attenuator factor β depends only on the temperature, which is monitored. The signal present at RD is $V_R = \beta V_1$. The voltage measured at every monitoring node i on the PCBs is $V_{Ci} = \alpha_i V_B$. The ratio V_{Ci}/V_R equals α_i/β, and is independent of the input voltage V_1. We can take the average $\langle V_{Ci}/V_R \rangle = \langle \alpha \rangle / \beta$, and define the calibration coefficients $\gamma_i = (\langle V_{Ci}/V_R \rangle)/(V_{Ci}/V_R) = \langle \alpha \rangle / \alpha_i$.

By multiplying the measured V_{Ci} by the corresponding γ_i, an improvement in the absolute accuracy by a factor of $\sqrt{N}$ can be obtained ($\approx \pm 0.1\%$), where N is the number of half-columns tested.

The distribution of the γ_i-normalized measured voltages, Fig. 4, is now very narrow. The maximum error observed is less than $\pm 0.06\%$. The same compensation procedure was also applied to the monitoring system of V_2 and V_3, obtaining similar performances, although slightly degraded by the additional splitter accuracy. The described calibration method gives a precision in the characterization of the difference (V_1–V_2), nominally 300 V, in the volt range. This accuracy is very important for the control of the demagnification factor within the HPDs [1] during data taking.

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